Anritsu Advancing beyond

Signal Quality Analyzer-R

MP1900A

SQA-R

Signal Quality Analyzer-R MP1900A

Due to the explosive growth of data traffic resulting from the popularity of smartphones and mobile terminals, network interfaces are transitioning to faster 200/400 GbE standards, and PCI bus interface speeds now exceed 10G. In addition, the equipment and chipsets using these interfaces support multi-channels and multi-protocols.
The MP1900A series is a high-performance BERT with excellent expandability for supporting Physical layer evaluations of these high-speed interfaces. The all-in-one design is ideal for early stage R&D evaluations of all interfaces covering next-generation Ethernet networks to bus interconnects

Model/Order Number, Name, Option

Model/Order No.	Name
MP1900A	Signal Quality Analyzer-R
MP1900A-110	Windows10 Upgrade Retrofit*1
MP1900A-ES310	Three Years Extended Warranty Service
MP1900A-ES510	Five Years Extended Warranty Service
MU195020A	21G/32G bit/s SI PPG
MU195020A-001	32 Gbit/s Extension
MU195020A-010	1ch Data Output
MU195020A-020	2ch Data Output
MU195020A-011	1ch 10Tap Emphasis
MU195020A-021	2ch 10Tap Emphasis
MU195020A-030	1ch Data Delay
MU195020A-031	2ch Data Delay
MU195020A-040	1ch Variable ISI
MU195020A-041	2ch Variable ISI
MU195020A-050	Sequence Editor Function
MU195020A-051	Sequence Editor Function PCIe 5 Extension
MU195020A-101	32 Gbit/s Extension Retrofit
MU195020A-111	1ch 10Tap Emphasis Retrofit
MU195020A-121	2ch 10Tap Emphasis Retrofit
MU195020A-130	1ch Data Delay Retrofit
MU195020A-131	2ch Data Delay Retrofit
MU195020A-140	1ch Variable ISI Retrofit
MU195020A-141	2ch Variable ISI Retrofit
MU195020A-340	1ch Variable ISI Retrofit
MU195020A-341	2ch Variable ISI Retrofit
MU195020A-350	Sequence Editor Function Retrofit
MU195020A-351	Sequence Editor Function PCIe 5 Extension Retrofit
MU195020A-ES310	Three Years Extended Warranty Service
MU195020A-ES510	Five Years Extended Warranty Service
MU195040A	21G/32G bit/s SI ED
MU195040A-001	32 Gbit/s Extension
MU195040A-010	1ch ED
MU195040A-020	2ch ED
MU195040A-011	1ch CTLE
MU195040A-021	2ch CTLE
MU195040A-022	Clock Recovery
MU195040A-101	32 Gbit/s Extension Retrofit
MU195040A-111	1ch CTLE Retrofit
MU195040A-121	2ch CTLE Retrofit
MU195040A-122	Clock Recovery Retrofit
MU195040A-ES310	Three Years Extended Warranty Service
MU195040A-ES510	Five Years Extended Warranty Service
MU196020C	PAM4 PPG
MU196020C-001	32G baud
MU196020C-002	58G baud
MU196020C-003	64G baud
MU196020C-011	4Tap Emphasis
MU196020C-030	Data Delay
MU196020C-040	Adjustable ISI
MU196020C-042	FEC Pattern Generation
MU196020C-043	FEC Error Insertion for PCIe6
MU196020C-045	USB4 Gen4 Pattern Generation
MU196020C-050	Inter-Module Synchronization

*1: This Windows 10 upgrade option is for MP1900A with Windows Embedded Standard 7 orders received before June 2020. It is performed by modifying hardware. We will dispose of any unnecessary Windows Embedded Standard 7 parts after the modification. Please contact our sales representative for details.

Model/Order No.	Name
MU196020C-112	32G to 58G baud Retrofit
MU196020C-113	32G to 64G baud Retrofit
MU196020C-123	58G to 64G baud Retrofit
MU196020C-111	4Tap Emphasis Retrofit
MU196020C-130	Data Delay Retrofit
MU196020C-140	Adjustable ISI Retrofit
MU196020C-142	FEC Pattern Generation Retrofit
MU196020C-143	FEC Error Insertion for PCIe6 Retrofit
MU196020C-145	USB4 Gen4 Pattern Generation Retrofit
MU196020C-150	Inter-Module Synchronization Retrofit
MU196020C-340	Adjustable ISI Retrofit
MU196020C-342	FEC Pattern Generation Retrofit
MU196020C-343	FEC Error Insertion for PCIe6 Retrofit
MU196020C-345	USB4 Gen4 Pattern Generation Retrofit
MU196020C-ES310	Three Years Extended Warranty Service
MU196020C-ES510	Five Years Extended Warranty Service
MU196020A	PAM4 PPG
MU196020A-001	32G baud
MU196020A-002	58G baud
MU196020A-003	64G baud
MU196020A-011	4Tap Emphasis
MU196020A-030	Data Delay
MU196020A-040	Adjustable ISI
MU196020A-042	FEC Pattern Generation
MU196020A-043	FEC Error Insertion for PCIe6
MU196020A-045	USB4 Gen4 Pattern Generation
MU196020A-050	Inter-Module Synchronization
MU196020A-051	Sequence Editor Function
MU196020A-052	Sequence Editor Function for Multi-channel
MU196020A-056	Sequence Editor Function PCIe 6 and CXL 3 Flits Extension
MU196020A-060	PCIe6 LEQ
MU196020A-112	32G to 58G baud Extension Retrofit
MU196020A-113	32G to 64G baud Retrofit
MU196020A-123	58G to 64G baud Retrofit
MU196020A-111	4Tap Emphasis Retrofit
MU196020A-130	Data Delay Retrofit
MU196020A-140	Adjustable ISI Retrofit
MU196020A-142	FEC Pattern Generation Retrofit
MU196020A-145	USB4 Gen4 Pattern Generation Retrofit
MU196020A-150	Inter-Module Synchronization Retrofit
MU196020A-156	Sequence Editor Function PCIe 6 and CXL 3 Flits Extension Retrofit
MU196020A-160	PCIe6 LEQ Retrofit
MU196020A-340	Adjustable ISI Retrofit
MU196020A-342	FEC Pattern Generation Retrofit
MU196020A-343	FEC Error Insertion for PCIe6 Retrofit
MU196020A-345	USB4 Gen4 Pattern Generation Retrofit
MU196020A-351	Sequence Editor Function Retrofit
MU196020A-352	Sequence Editor Function for Multi-channel Retrofit
MU196020A-356	Sequence Editor Function PCIe 6 and CXL 3 Flits Extension Retrofit
MU196020A-360*2	PCIe6 LEQ Retrofit
MU196020A-ES310	Three Years Extended Warranty Service
MU196020A-ES510	Five Years Extended Warranty Service

*2: This option is supported in accordance with the MU196020A serial number. For details, contact our sales representative.

Model/Order No.	Name
MU196040B	PAM4 ED
MU196040B-001	32G baud (2.4G to 32.1G)
MU196040B-002	58G baud (NRZ: 2.4G to 64.2G, PAM4: 2.4G to 58.2G)
MU196040B-005	64G baud*3
MU196040B-011	Equalizer
MU196040B-021	29G baud Clock Recovery (2.4G to 29G)
MU196040B-022	32G baud Clock Recovery (2.4G to 32.1G)
MU196040B-023	58G baud Clock Recovery Extension (51G to 58.2G)
MU196040B-041	SER Measurement
MU196040B-042	FEC Analysis
MU196040B-043	FEC Analysis for PCIe6
MU196040B-051	PCIe Sequence Editor Pattern Analysis
MU196040B-111	Equalizer Retrofit
MU196040B-112	32G to 58G baud Extension Retrofit
MU196040B-115	32G to 64G baud Extension Retrofit*3
MU196040B-121	29G baud Clock Recovery Retrofit
MU196040B-122	32G baud Clock Recovery Retrofit
MU196040B-123	58G baud Clock Recovery Extension Retrofit
MU196040B-124	32G baud Clock Recovery Extension Retrofit
MU196040B-125	58G to 64G baud Extension Retrofit*3
MU196040B-141	SER Measurement Retrofit
MU196040B-341	SER Measurement Retrofit
MU196040B-342	FEC Analysis Retrofit
MU196040B-343	FEC Analysis for PCIe6 Retrofit
MU196040B-351	PCIe Sequence Editor Pattern Analysis Retrofit
MU196040B-ES310	Three Years Extended Warranty Service
MU196040B-ES510	Five Years Extended Warranty Service
MU196040A	PAM4 ED
MU196040A-001	32.1G baud Decoder
MU196040A-022	25.5G to 32.1G baud Clock Recovery
MU196040A-041	SER Measurement
MU196040A-122	25.5G to 32.1G baud Clock Recovery Retrofit
MU196040A-141	SER Measurement Retrofit
MU196040A-ES310	Three Years Extended Warranty Service
MU196040A-ES510	Five Years Extended Warranty Service
MU196050B	Noise Generator
MU196050B-ES310	Three Years Extended Warranty Service
MU196050B-ES510	Five Years Extended Warranty Service
MU195050A	Noise Generator
MU195050A-001	White Noise
MU195050A-101	White Noise Retrofit
MU195050A-ES310	Three Years Extended Warranty Service
MU195050A-ES510	Five Years Extended Warranty Service
MU196060A	32G baud NRZ/PAM4 Re-Driver
MU196060A-001	Clock Recovery for SSC
MU196060A-301	Clock Recovery for SSC Retrofit
MU196060A-ES310	Three Years Extended Warranty Service
MU196060A-ES510	Five Years Extended Warranty Service

*3: There are software restrictions when using 64G baud.
For details, consult our business sales representative.

Model/Order No.	Name
MU191000A	Synthesizer
MU191000A-ES310	Three Years Extended Warranty Service
MU191000A-ES510	Five Years Extended Warranty Service
MU181000B	12.5 GHz 4port Synthesizer
MU181000B-002	SSC Extension
MU181000B-102	SSC Extension Retrofit
MU181000B-ES310	Three Years Extended Warranty Service
MU181000B-ES510	Five Years Extended Warranty Service
MU181500B	Jitter Modulation Source
MU181500B-ES310	Three Years Extended Warranty Service
MU181500B-ES510	Five Years Extended Warranty Service
MX183000A	High-Speed Serial Data Test Software
MX183000A-PL001	Jitter Tolerance Test
MX183000A-PL011	PCIe Link Sequence
MX183000A-PL021	PCIe Link Training
MX183000A-PL022	USB Link Training
MX183000A-PL023	USB 3.2 × 2 Link Training
MX183000A-PL025	PCIe 5 Link Training
MX183000A-PL026	PCIe 6 Link Training
MX183000A-PL031	DUT Error Counts Import

Signal Quality Analyzer-R MP1900A Main Frame Specifications

Functions	
Input Device, Button	Resistance film touch panel, Rotary encoder, Function button, Power button
LED	Power, Power Stan dBy, Disk Access
LCD	12.1 inch WXGA (1280 × 800)
Ethernet	10/100/1000 Base-T RJ45 1 port (External: For remote control) 10/100/1000 Base-T RJ45 1 port (Internal: Reserved for future use)
External Display	D-Sub 15 pin 1 port HDMI Type A 1 port
USB	Front panel USB Type A 4 port Rear panel USB Type A 2 port
Rear Panel	1 port (For remote control)
Module Slot	8 Slots
Functional Earth Terminal	Front panel: 2 Jacks Rear panel: 1 Terminal
OS	Windows 10
Internal Storage Device	SATA 2.5-inch HDD 1 Unit (tray loading)*1
Remote Interface	GPIB, Ethernet External (automatic switchover)
Internal Reference Clock	10 MHz ± 1 ppm (Accuracy at initial shipment)
Environmental Performance	
Power Supply*2	100 V(ac) to 120 V(ac), 200 V(ac) to 240 V(ac) (automatic switching between 100 and 200 V systems), 50 Hz to 60 Hz
Power Consumption	1350 VA
Operating Temperature Range	+5°C to +40°C
Dimensions and Mass	340 (W) × 222.5 (H) × 451 (D) mm (Protrusions excluded) 20 kg (excluding modules, blank panels, protective cover, power cord)
CE	
EMC	2014/30/EU, EN61326-1, EN61000-3-2
LVD	2014/35/EU, EN61010-1
RoHS	2011/65/EU, (EU) 2015/863, EN IEC 63000: 2018
UKCA	
EMC	S.I. 2016 No.1091, EN 61326-1, EN61000-3-2
LVD	S.I. 2016 No.1101, EN 61010-1
RoHS	S.I. 2012 No.3032, EN IEC 63000: 2018

*1: Removing and replacing the HDD by Customer is outside the scope of warranty coverage.
*2: Operating voltage is –10% to +10% of rated voltage

SI PPG MU195020A Specifications

Operating Bit Rate

<table>
<tr><td>Bit Rate Setting Range
(MU181000B synchronized operation)</td><td>2.400 000 Gbit/s to 21.000 000 Gbit/s, 0.000 002 Gbit/s step*1
2.400 000 Gbit/s to 25.000 000 Gbit/s, 0.000 002 Gbit/s step*2
25.000 004 Gbit/s to 32.100 000 Gbit/s, 0.000 004 Gbit/s step*2
Offset
–1000 to +1000 ppm, 1 ppm step*3</td></tr>
<tr><td>Bit Rate Setting Range
(MU181500B synchronized operation)</td><td>2.400 000 Gbit/s to 3.125 000 Gbit/s, 0.000 002 Gbit/s step
3.200 002 Gbit/s to 6.250 000 Gbit/s, 0.000 002 Gbit/s step
6.400 002 Gbit/s to 12.500 000 Gbit/s, 0.000 002 Gbit/s step
12.800 002 Gbit/s to 21.000 000 Gbit/s, 0.000 002 Gbit/s step*1
12.800 002 Gbit/s to 25.000 000 Gbit/s, 0.000 002 Gbit/s step*2
25.600 004 Gbit/s to 32.100 000 Gbit/s, 0.000 004 Gbit/s step*2
Offset
–1000 to +1000 ppm, 1 ppm step*3</td></tr>
<tr><td>Bit Rate Setting Range
(with external clock source)</td><td>When the Output Clock Rate is set to Full Rate
<table>
<tr><th>Operating
Bit Rate Range</th><th>Input Clock
Frequency</th><th>Relationship between Bit
Rate and Clock Frequency</th></tr>
<tr><td>2.4 Gbit/s to 16.0 Gbit/s</td><td>2.4 GHz to 16.0 GHz</td><td>Operate at 1/1 clock</td></tr>
<tr><td>16.0 Gbit/s to 20.0 Gbit/s*1</td><td>8.0 GHz to 10.0 GHz</td><td>Operate at 1/2 clock</td></tr>
<tr><td>20.0 Gbit/s to 21.0 Gbit/s*1</td><td>10.0 GHz to 10.5 GHz</td><td>Operate at 1/2 clock</td></tr>
<tr><td>16.0 Gbit/s to 21.0 Gbit/s*2</td><td>8.0 GHz to 10.0 GHz</td><td>Operate at 1/2 clock</td></tr>
<tr><td>20.0 Gbit/s to 32.1 Gbit/s*2</td><td>10.0 GHz to 16.05 GHz</td><td>Operate at 1/2 clock</td></tr>
<tr><td>25.0 Gbit/s to 32.1 Gbit/s*2</td><td>6.25 GHz to 8.025 GHz</td><td>Operate at 1/4 clock</td></tr>
</table>
When the Output Clock Rate is set to Half Rate
<table>
<tr><th>Operating
Bit Rate Range</th><th>Input Clock
Frequency</th><th>Relationship between Bit
Rate and Clock Frequency</th></tr>
<tr><td>2.4 Gbit/s to 28.1 Gbit/s*1</td><td>1.2 GHz to 14.05 GHz</td><td>Operate at 1/2 clock</td></tr>
<tr><td>2.4 Gbit/s to 32.1 Gbit/s*2</td><td>1.2 GHz to 16.05 GHz</td><td>Operate at 1/2 clock</td></tr>
<tr><td>25.0 Gbit/s to 32.1 Gbit/s*2</td><td>6.25 GHz to 8.025 GHz</td><td>Operate at 1/4 clock</td></tr>
</table></td></tr>
<tr><td>Bit Rate Setting Range
(MU181500B synchronized operation
with external clock source)</td><td>When the Output Clock Rate is set to Full Rate
<table>
<tr><th>Operating
Bit Rate Range</th><th>Input Clock
Frequency</th><th>Relationship between Bit
Rate and Clock Frequency</th></tr>
<tr><td>2.4 Gbit/s to 15.0 Gbit/s</td><td>2.4 GHz to 15.0 GHz</td><td>Operate at 1/1 clock</td></tr>
<tr><td>15.0 Gbit/s to 20.0 Gbit/s*1</td><td>7.5 GHz to 10.0 GHz</td><td>Operate at 1/2 clock</td></tr>
<tr><td>20.0 Gbit/s to 21.0 Gbit/s*1</td><td>10.0 GHz to 10.5 GHz</td><td>Operate at 1/2 clock</td></tr>
<tr><td>15.0 Gbit/s to 20.0 Gbit/s*2</td><td>7.5 GHz to 10.0 GHz</td><td>Operate at 1/2 clock</td></tr>
<tr><td>20.0 Gbit/s to 30.0 Gbit/s*2</td><td>10.0 GHz to 15.0 GHz</td><td>Operate at 1/2 clock</td></tr>
<tr><td>25.0 Gbit/s to 32.1 Gbit/s*2</td><td>6.25 GHz to 8.025 GHz</td><td>Operate at 1/4 clock</td></tr>
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When the Output Clock Rate is set to Half Rate
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<tr><td>2.4 Gbit/s to 21.0 Gbit/s*1</td><td>1.2 GHz to 10.5 GHz</td><td>Operate at 1/2 clock</td></tr>
<tr><td>2.4 Gbit/s to 30.0 Gbit/s*2</td><td>1.2 GHz to 15.0 GHz</td><td>Operate at 1/2 clock</td></tr>
<tr><td>25.0 Gbit/s to 32.1 Gbit/s*2</td><td>6.25 GHz to 8.025 GHz</td><td>Operate at 1/4 clock</td></tr>
</table></td></tr>
</table>

*1: Not available Option x01
*2: Available Option x01
*3: Offset setting range depends on the bit rate. The range is -1000 to 0 ppm at the following bit rate.
Full Rate: 12.500000 Gbit/s, 25.000000 Gbit/s
Half Rate: 25.000000 Gbit/s

External Clock Input

Number of Input	1 (Single-end)
Input Frequency Range	1.2 GHz to 16.05 GHz
Input Amplitude	0.3 Vp-p to 1.0 Vp-p (–6.5 to +4.0 dBm)
Termination	AC, 50Ω
Connector	SMA (f)

Aux Input and Output

Aux Input	
Number of Input	1 (Single-end)
Signal Type	Error Injection, Burst, Sequence Trigger*
Minimum Pulse Width	1/128 of data rate
Input Level	• 0/–1 V (H: –0.25 V to 0.05 V, L: –1.1 V to –0.8 V) • 0/–0.5 V (H: –0.05 V to 0.05 V, L: –0.55 V to –0.45 V) Select one of the above.
Termination	GND, 50Ω
Connector	SMA (f)
Aux Output	
Number of Output	2 (Differential)
Signal Type	1/n Clock (n = 4, 6, 8, 10 ... 510, 512), Pattern Sync, Burst Out2, LTSSM Trigger*
Output Level	0/–0.6 V (H: –0.25 V to 0.05 V, L: –0.80 V to –0.45 V)
Terminator	GND, 50Ω
Connector	SMA (f)

*: Sequence Trigger and LTSSM Trigger can be selected only when Test Pattern is Sequence.

Gating Output

Number of Output	2 (Differential)
Signal Type	Burst, Repeat, LFPS*1
Output Level	0/–1 V (H: –0.25 V to 0.05 V, L: –1.25 V to –0.8 V)*2
Terminator	GND, 50Ω
Connector	SMA (f)

*1: Can be set when Test Pattern is Sequence and Specification is USB3.0 or USB3.1 Gen2.
*2: L: Output Enable, H: Output Disable

Generated Pattern*1

PRBS	
Pattern Length	$2^n - 1$ (n = 7, 9, 10, 11, 15, 20, 23, 31)
Mark Ratio	1/2 (1/2INV is supported by a logical inversion.)
Zero-Substitution	
Additional Bit	0 bit, 1 bit
Pattern Length	2^n or $2^n - 1$ (n = 7, 9, 10, 11, 15, 20, 23)
Start Position	Substitutes the bit coming after the maximum "0" successive bits.
Length of Consecutive Zero Bits	1 to (Pattern Length – 1) bits If the bit coming after Zero-substitution is "0", then it is replaced with "1".
Data	
Data Length	2 bits to 268435456 bits, 1 bit step
Current Outputting Pattern	1 to 10, 1 step Outputs the pattern of the selected number. Patterns can be switched glitch-free.
Mixed Pattern	
Pattern	Data
Mixed Block	To the smaller of the following values: 1 to 511 Block, 1 Block step $\mathrm{INT}\left(\frac{268435456}{\text{ROW count}} \times \text{Data length}\right)$ bits $\mathrm{INT}\left(\frac{268435456 + 2^{31}}{\text{ROW length}} \times \text{ROW count}\right)$ bits
Mixed Row Length	2048 to 268435456 + 2^{31} bits, 1024 bits step (Data + PRBS Length)
Data Length	1024 bits to 268435456 bits, 1 bit step
Number of Rows	1 to 16, 1 step
Number of Blocks	1 to 511, 1 step
PRBS Pattern Length, Mark Ratio	Same as PRBS.
PRBS Sequence	Restart, Consecutive
Scramble	Can be set per PRBS and Data for each Block (except the Data area for Block 1)
PAM4*2	
Pattern Type	Square Wave, JP03A, JP03B, PRQS10, SSPR, QPRBS13, QPRBS13-CEI, SSPRQ, Transmitter Linearity, PRBS13Q, PRBS31Q, User Define
User Define in detail	Raw Data: PRBS, Data PRBS Stage: Same as PRBS PRBS Inversion: Logic Inversion/Non-Inversion of PRBS part Data Length: Same as Data Gray Coding: Gray Coding ON/OFF
Sequence*3	
Specification	PCIe1, PCIe2, PCIe3, PCIe4, PCIe5*4, USB3.0, USB3.1 Gen2
Transmit	Starts transmitting the sequence pattern.
Manual	Enabled when Manual Trigger is set.
Trigger Block No.	Sets the block number of the sequence to output an LTSSM Trigger signal from AUX Output connector. 1 to 128 Block No., 1 step

*1: Since the output circuit is DC-terminated using the AC-coupled Bias Tee method, the same symbol pattern has a 50% change in output level over a continuous period of about 5 µs.
*2: Configurable when 2ch Combination or 64G × 2ch Combination is set.
*3: The MU195020A-z50 is required. This can be set only when Module Combination is set to Independent.
If either Ch1 or Ch2 is set to Sequence, the other is also set to Sequence.
*4: Requires both MU195020A-050/350 and MU195020A-051/351 options.

SI PPG MU195020A Specifications

Pattern Sequence

Repeat	Continuous Pattern
Burst	
Burst Cycle	25600 bits to 2147483648 bits, 1024 bits step
Enable period	Internal: 12800 bits to 2147483392 bits, 256 bits step Ext Trigger: 12800 bits to 2147483648 bits, 256 bits step

Pre-Code

The function is available only when Pattern Sequence is Repeat.

Modulation Type	2ch Combination: DQPSK
Initial Data	Choose 0 or 1.

Error addition

Area	ALL, Specific Block (Can be selected only for Mixed.)
Internal Trigger	
Error Variation	Repeat, Single
Error Ratio	*E – n (*= 1 to 9, n = 3 to 12), Upper limit is 5E–3
External Trigger*	
Control Method	External-Trigger (Rise edge trigger), External-Disable (L: Disable)
Bit/Burst	Selects Bit Error or Burst Error
Burst Length	1 to 127, 1 step

*: Can be set when Test Pattern is other than Sequence.

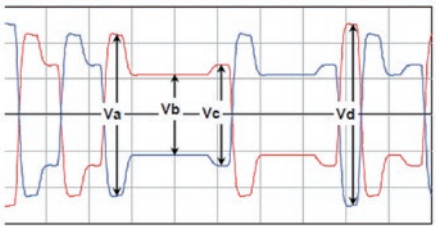
Data Output

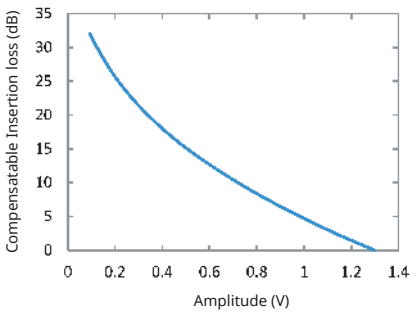
Unless otherwise specified, these are defined with the conditions of PRBS $2^{31} – 1$, Mark ratio 1/2, and Cross Point 50%.
These values are monitored using an applicable part (Coaxial Cable J1439A, 0.8 m, K connector) at a sampling oscilloscope bandwidth of 70 GHz.

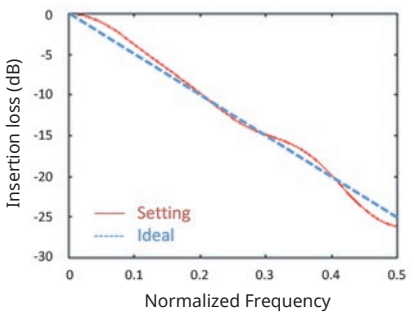
Number of Outputs	Option x10: 2 (Data, $\overline{\text{Data}}$) Option x20: 4 (Data1, $\overline{\text{Data}}$1, Data2, $\overline{\text{Data}}$2)
Output Amplitude	
Setting Range	0.1 Vp-p to 1.3 Vp-p, 2 mV step
Setting Error	±50 mV ±17%
Offset	
Setting Range	$-2.0 - \frac{\text{Amp.}}{2}$ to $+3.3 - \frac{\text{Amp.}}{2}$ Vth, 1 mV step
Setting Error	±65 mV ±10% of offset (Vth) ± (Eye Amp. Accuracy/2)*1
Defined Interface	NECL, SCFL, NCML, PCML, LVPECL
Cross Point	50% Fixed
Rising/Falling Time	20 to 80%*1, *2, 12 ps (typ.), ≤15 ps
Half Period Jitter	
Setting Range	–20 to 20, 1 step
Setting Error	±0.02 UI (typ.)*3
Jitter (typ.)	Peak-to-Peak Jitter (p-p): 6 ps p-p (Measurement count 30) (typ.)*2, *4 Random Jitter (RMS): 300 fs rms (1,0 repeat pattern) (typ.)*2, *4 Random Jitter (RMS): 115 fs rms (28 Gbit/s 1,0 repeat pattern) (typ.)*2, *5 Total Jitter (Total): 6 ps (Measurement count 30) (typ.)*2, *4, *6
Waveform Distortion (0-peak)	±25 mV ±15% (typ.)*2
Data/$\overline{\text{Data}}$ Skew	±1 ps (typ.)*7, *8
Skew Between Channels*9	±0.25 UI*8
Termination	AC, DC switching, 50Ω For DC*10: GND, –2 V, +1.3 V, +3.3 V, Open (LVDS)
Connector	K (f)

*1: Option x11 or Option x21 is installed and that Emphasis is not set.
*2: If Option x01 is not available, then this is at 21 Gbit/s.
If Option x01 is available, then this is at 32.1 Gbit/s.
Amplitude: 1.0 Vp-p
*3: When the value is set to 0.
*4: Using oscilloscope with residual jitter of less than 200 fs rms.
*5: Using oscilloscope with residual jitter of less than 70 fs rms.
*6: Defined by PRBS $2^{15} – 1$, BER 10^{-12}.
*7: Cable error is not included.
*8: Includes standard accessory Coaxial Adapter J1359A (K-P.K-J to SMA).
*9: When Option x20 is available.
*10: The output circuit is DC-terminated using the AC-coupled Bias Tee.

10Tap Emphasis (Option 011 or 021)

Emphasis Tap	10 (6 post-cursor, 3 pre-cursor)
Cursor Setting Range	–20 to +20 dB, 0.1 dB step Post-Cursol: $20\log_{10}(\frac{V_a}{V_b})$, Pre-Cursol: $20\log_{10}(\frac{V_c}{V_b})$ 
Accuracy	±1 dB (typ., Defined for the preset of 8, 16, and 25 Gbit/s for PCIe 3 and PCIe 4 respectively)
Emphasis Peak Voltage Setting Range	0.1 Vp-p to 1.5 Vp-p (Single-end)
Transition Time from Idle State	≤8 ns (Maximum time to transition to valid diff signaling after leaving Electrical Idle)

Channel Emulator (Option 040 or 041)	Normal: Outputs signal emulating transmission channel equivalent to read S-parameter at PPG Data Output Inverse: Outputs signal with set De-Emphasis for compensating for transmission channel loss equivalent to read S-parameter at PPG Data Output The following graph indicates the maximum transmission channel loss that can be compensated for using the Channel Emulator function without causing a decrease in Amplitude. 
Response	Normal, Inverse
S-Parameter file	S2P File (extension *.s2p), S4P File (Input ports 1 and 3; Output ports 3 and 4, extension *.s4p) Supports Vector Network Analyzer MS4640B Series output files

Variable ISI (Option 040 or 041)	Sets ISI-generated channel loss and outputs this emulated waveform at PPG output Data signal (Output waveform amplitude standardized as set amplitude) Used in combination with Channel Board, such as J1758 (Optional Accessory)
Frequency Setting	Can set Insertion Loss at Nyquist or 1/2 Nyquist frequency
Insertion Loss Setting	1.5 to 25 dB 0.01 dB step @Nyquist Frequency 0 to 25 dB 0.01 dB step @1/2Nyquist Frequency
Insertion Loss Accuracy	±1 dB nominal (design guarantee) at Nyquist frequency, 10 dB, with 1,0 pattern repetition ±1 dB nominal (design guarantee) at 1/2 Nyquist frequency 5 dB, with 1, 1, 0, 0 pattern repetition Bit rates of 16 Gbit/s, 25 Gbit/s (Option 01 installed), Eye Amplitude of 1.0 Vp-p, each spectrum The Insertion Loss Accuracy is shown by the following graph of the frequency characteristics when 25 dB and 12.5 dB is set at the Nyquist frequency and 1/2 Nyquist frequency, respectively. (ISI Nominal Data) 
Emulator On/Off	Can be composed of each Channel Emulator, Variable ISI, and Emphasis Tap

SI PPG MU195020A Specifications

Clock Output

These values are monitored using an applicable part (Coaxial Cable J1439A, 0.8 m, K connector) at a sampling oscilloscope bandwidth of 70 GHz.

Frequency	
Full Rate	2.4 GHz to 21.0 GHz*1 2.4 GHz to 32.1 GHz*2 Operation bit rate is same as clock output frequency.
Half Rate	1.2 GHz to 10.5 GHz*1 1.2 GHz to 16.05 GHz*2 Operation bit rate is double of output clock frequency.
Number of Output	1
Amplitude	0.3 Vp-p to 1.0 Vp-p
Termination	AC, 50Ω
Connector	K (f)

*1: Option x01 not available.
*2: Option x01 available.

Data Delay

When Option x30 or Option x31 is available.

Phase Variable Range	–1000 mUI to +1000 mUI, 2 mUI step
Phase Setting Error	±50 m UIp-p (typ.)*
Calibration Indicator	This indicator is on when Calibration is required due to: • 1/1 Clock frequency change by ±250 kHz. • Ambient temperature change by ±5 degree.

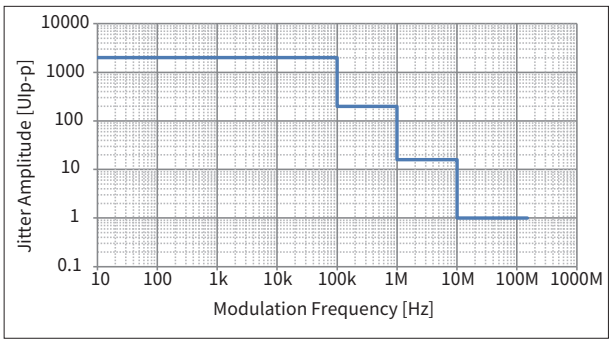
*: When using an item with an oscilloscope residual jitter of less than 200 fs rms.

Jitter Setting Range

Jitter Setting Range

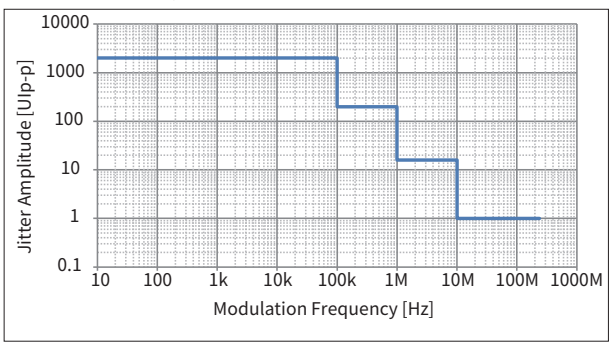
When linking with MU181000A/B and MU181500B
SJ1 Clock Output Rate
At Half Rate

30 < Bit rate ≤ 32.1 Gbit/s, 8 < Bit rate ≤ 17 Gbit/s



Modulation Frequency [Hz]	Jitter Amplitude [UIp-p]
10 to 100k	0 to 2000
100.1k to 1M	0 to 200
1.001M to 10M	0 to 16
10.01M to 150M	0 to 1

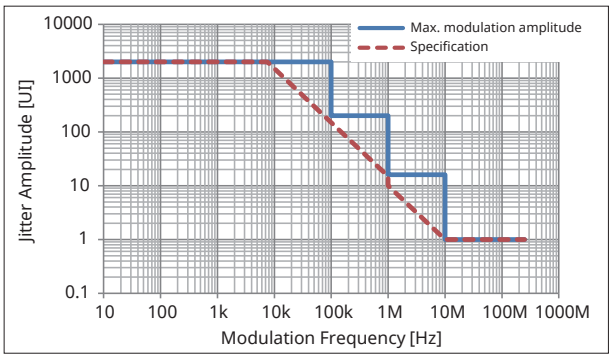
17 < Bit rate ≤ 30 Gbit/s



Modulation Frequency [Hz]	Jitter Amplitude [UIp-p]
10 to 100k	0 to 2000
100.1k to 1M	0 to 200
1.001M to 10M	0 to 16
10.01M to 250M	0 to 1

Jitter Tolerance

Jitter Tolerance Mask*	Bit rate: 16, 28.1*, 32.1 Gbit/s* Pattern: PRBS $2^{31} - 1$ SSC with a 5300 ppm amplitude and RJ of 0.3 UI can be simultaneously applied by using MU181500B. These specifications are defined assuming the following conditions: Loopback connection to the MU195040A, defined by one specific temperature in the range of 20°C to 30°C. When RJ + BUJ is bigger than 0.5 UIp-p or SJ + RJ + BUJ is bigger than the standard value + 0.3 UIp-p, "Overload" is displayed on the MU181500B screen. The maximum applied modulation jitter depends on the bit rate. Refer to the jitter setting range for details.



Modulation Frequency [Hz]	Max. Modulation Amplitude [UIp-p]	Specification [UIp-p]
10	2,000	2,000
7,500	2,000	2,000
100,000	2,000	150
1,000,000	200	15
10,000,000	16	1
250,000,000	1	1

*: Option x01 available.

Multichannel Operation

Combination Setting*1, *2	
2ch Combination	Alternately outputs each bit in pattern as 32/64 Gbit/s band signal source to two channels.
Channel Synchronization*1	Number of channels: 2
Combination of Modules	Slot 1 to 4: 2-channel combination, channel synchronization*3
2-channel synchronization	
Output	Phase variable range –64 000 mUI to +64 000 mUI*4 Phase variable step 2 mUI*4
Pattern	
Data	Data Length 2 × n to 268435456 × n bits, n bits step*5
Mixed	Row Length (2048 × n) to { (268435456 + 2^{31}) × n }, (1024 × n) bits step*5 Data Length (1024 × n) to 268435456 × n bits, n bits step*5

*1: Option x31 is required for target channels. Multichannel operation cannot be set when Test Pattern is set to Sequence.
*2: Combination extending over multiple slots cannot be set.
*3: When the options in the modules are the same and they are installed sequentially from slot 1,
*4: A separate value can be set for each channel. This value is common to both Channel Combination and Channel Synchronization.
*5: Common to every channel specified by Combination Setting.

Extension Function

PAM4	Supports the following by combining MU195020A with MZ1834A/B and G0375A. PAM4 signal generation • Amplitude (Single-end) 0.048 to 0.310 Vp-p (MZ1834A) • Amplitude (Single-end) 0.048 to 0.489 Vp-p (MZ1834B) • Amplitude (Single-end) 0.3 to 1.95 Vp-p (G0375A) PAM4 Emphasis signal generation (when Option x11 or Option x21 is installed) • Emphasis Peak Voltage (Single-end) 0.048 to 0.357 Vp-p (MZ1834A) • Emphasis Peak Voltage (Single-end) 0.048 to 0.564 Vp-p (MZ1834B) • Emphasis Peak Voltage (Single-end) 0.3 to 2.25 Vp-p (G0375A)

Operating Bit Rate

Operating Bit Rate	2.4 Gbit/s to 21.0 Gbit/s*1 2.4 Gbit/s to 32.1 Gbit/s*2

*1: Option x01 not available
*2: Option x01 available

System Clock

System Clock	External, Clock Recovery, Clock and Data Recovery*1, *2

*1: Available when Option x22 is installed. If it is not installed, only External is available.
*2: After implementing Option x22, the Clock is recovered from the data input to the Data1

Data Input

Number of Inputs	2 (Data, $\overline{\text{Data}}$) (Differential)*1 4 (Data1, $\overline{\text{Data1}}$, Data2, $\overline{\text{Data2}}$) (Differential)*2
Amplifier	Single-end 50Ω, Differential 50Ω, Differential 100Ω can be set. At Single-end 50Ω: Data and $\overline{\text{Data}}$ can be set. At differential 50/100Ω: Tracking, Independent, Alternate can be set. When Alternate is selected: Data-$\overline{\text{Data}}$ and $\overline{\text{Data}}$-Data can be set.*3 CTLE: On/Off Switching*4
Input Signal Format	NRZ, PAM4
Input Amplitude*5	0.05 Vp-p to 1.0 Vp-p (NRZ) 0.3 Vp-p to 1.0 Vp-p (PAM4, ≤ 28.1 Gbaud) 0.4 Vp-p to 1.0 Vp-p (PAM4, > 28.1 Gbaud)
Threshold Voltage	–3.5 V to +3.3 V (1 mV step) (Can be set separately.) (Absolute value of difference between Data and $\overline{\text{Data}}$ Threshold values shall be 3 V or less.)
Input Sensitivity	NRZ*5, *6, *7

Bit Rate	21.0 Gbit/s	28.1 Gbit/s*8
Amplitude	19 mVp-p (typ.), ≤27 mVp-p	22 mVp-p (typ.), ≤31 mVp-p
Eye Height*9	13 mV (typ.)	15 mV (typ.)

PAM4*5, *7, *11

Baud Rate	21.0 Gbaud	28.1 Gbaud*8
Amplitude	120 mVp-p (typ.), 40 mV/Eye	150 mVp-p (typ.), 50 mV/Eye
Eye Height*9	24 mV (typ.)	26 mV (typ.)

Phase Margin — NRZ*6, *10

Bit Rate	21.0 Gbit/s	25.0 Gbit/s*8	28.1 Gbit/s*8	32.1 Gbit/s*8
Phase Margin	33 ps (typ.)	27 ps (typ.)	20 ps (typ.)	18 ps (typ.)

PAM4 Middle*11, *12

Baud Rate	21.0 Gbaud	25.0 Gbaud*8	28.1 Gbaud*8	32.1 Gbaud*8
Phase Margin	13 ps (typ.)	8 ps (typ.)	5 ps (typ.)	2 ps (typ.)
Eye Width	26.5 ps (typ.)	20 ps(typ.)	15 ps(typ.)	13 ps(typ.)

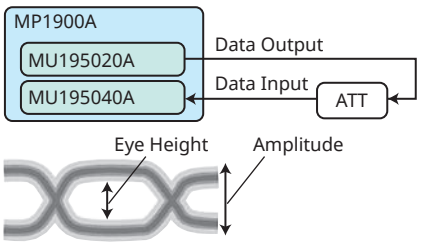
PAM4 Upper/Lower*11, *12

Baud Rate	21.0 Gbaud	25.0 Gbaud*8	28.1 Gbaud*8
Phase Margin	8 ps (typ.)	5 ps (typ.)	3 ps (typ.)
Eye Width	26.5 ps (typ.)	20 ps (typ.)	15 ps (typ.)

Termination	GND, Termination Variable Selectable 50Ω
Termination Voltage	Termination Variable Setting: –2.5 V to +3.5 V, 10 mV step
Connector	K (f)
CTLE*1	
Band	Off, 8 Gbit/s to 10 Gbit/s, 16 Gbit/s to 20 Gbit/s, 25 Gbit/s to 28 Gbit/s, PCIe3, PCIe4, PCIe5
Amplitude	0.05 Vp-p to 0.4 Vp-p (Input range not saturated when CTbE On)
CTLE Gain	Setting range 0 to –12 dB, 0.1 dB step Accuracy ±0.5 dB (typ.)

*1: Option x10
*2: Option x20
*3: Absolute value of difference between Data and $\overline{\text{Data}}$ Threshold values shall be 1.5 V or less.
*4: Option x11 or Option x21
*5: The Amplitude at NRZ input is the Auto Adjust function operation range. The Amplitude at PAM4 input is the PAM4 Auto Search function operation range. Input sensitivity is the minimum input amplitude which becomes error-free.
*6: PRBS 31, Single-end, Mark ratio 1/2, CTLE OFF
*7: Defined by one specific temperature in the range of 20°C to 30°C.
*8: Option x01

*9: Sensitivity of eye height.
Eye height is the minimum value that induces no bit error when MU195040A receives the output signal from MU195020A + ATT in the measurement system shown in the following figure (using a sampling oscilloscope of 70 GHz band or higher for measuring output amplitude)



*10: When using 0.5 Vp-p Input and External Clock.
*11: At PRBS15, Single-end, Mark Ratio 1/2 equivalent, and CTLE OFF, with MU195020A + G0375A
*12: At Emphasis ON (best value within range of 1Pre ≤ 3 dB/1Post ≤ 1 dB) based on IEEE802.3bs measurement method

Clock Input

Number of Inputs	1 (Single-end)
Frequency Range	1.2 GHz to 16.05 GHz
Input Level	0.3 Vp-p to 1.0 Vp-p (–6.5 to +4.0 dBm)
Termination	AC, 50Ω
Connector	SMA (f)

Aux Input, Aux Output

Aux Input	
Number of Inputs	1 (Single-end)
Input Signal	External Mask, Burst, Capture External Trigger
Minimum Pulse Width	1/128 of Data rate
Input Level	• 0/–1 V (H: –0.25 V to 0.05 V, L: –1.1 V to –0.8 V) • 0/–0.5 V (H: –0.05 V to 0.05 V, L: –0.55 V to –0.45 V) • V_{TH} 0 V (Input amplitude 0.5 Vp-p to 1.0 Vp-p) Select one of the above.
Termination	GND, 50Ω
Connector	SMA (f)
Aux Output	
Number of Outputs	2 (Differential)
Output Signal Selection	1/n Clock (n = 4, 6, 8, 10...510, 512), Pattern Sync*, Sync Gain, Error Output
Pattern Sync	PRBS, PRGM Position: 1 to (Least common multiple of Pattern Length' and 128) – 135, 8 step Pattern Length' shall be the value obtained by multiplying Pattern Length setting until it becomes 512 or more if it is 511 or less. Mixed Data Block No. setting: 1 to the Block No. specified for Mixed Data, in single steps Row No. setting: 1 to the Row No. specified for Mixed Data, in single steps
Output Level	0/–0.6 V (H: –0.25 V to 0.05 V, L: –0.80 V to –0.45 V)
Termination	GND, 50Ω
Connector	SMA (f)

*: Cannot be selected when Test Pattern is HSSB Data.

Pattern Detection

PRBS	
Pattern Length	$2^n – 1$ (n = 7, 9, 10, 11, 15, 20, 23, 31)
Mark Ratio	1/2 (1/2INV is supported by a logical inversion.)
Zero-Substitution	
Additional Bit	0 bit, 1 bit
Pattern Length	2^n or $2^n – 1$ (n = 7, 9, 10, 11, 15, 20, 23)
Start Position	Substitutes the bit coming after the maximum "0" successive bits.
Successive-zeros Bit Length	1 to (Pattern Length – 1) bits If the bit coming after Zero-substitution is "0," then it is replaced with "1."
Data	
Pattern Length	2 bits to 268435456 bits, 1 bit step

Mixed Pattern	
Pattern	Data
Mixed Block	To the smaller of the following values: 1 to 511 Block, 1 Block step $\mathrm{INT}\left(\frac{268435456}{\text{ROW count}} \times \text{Data length}\right)$ bits $\mathrm{INT}\left(\frac{268435456 + 2^{31}}{\text{ROW length}} \times \text{ROW count}\right)$ bits
Mixed Row Length	2048 to 268435456 + 2^{31} bits, 1024 bits step (Data + PRBS Length)
Pattern Length	1024 bits to 268435456 bits, 1 bit step
Number of Rows	1 to 16, 1 step
Number of Blocks	1 to 511, 1 step
PRBS Steps/Mark Ratio	Same as PRBS.
PRBS Sequence	Restart, Consecutive
Descramble	Can be set per PRBS and Data for each Block (except the Data area for Block 1).
PAM4*1	
Pattern Type	Square Wave, JP03A, JP03B, PRQS10, SSPR, QPRBS13, QPRBS13-CEI, SSPRQ, Transmitter Linearity, PRBS13Q, PRBS31Q, User Define
User Define in detail	Raw Data: PRBS, Data PRBS Stage: Same as PRBS PRBS Inversion: Logic Inversion/Non-Inversion of PRBS part Data Length: Same as Data Gray Coding: Gray Coding ON/OFF
HSSB Data*2	Specification PCIe1, PCIe2, PCIe3, PCIe4, PCIe5, USB3.0, USB3.1 Gen2

*1: Configurable when 2ch Combination is set.
*2: This can be set only when Module Combination is set to Independent and the channel is Data1.

Pattern Sequence

Sequence	Repeat, Burst
Repeat	Continuous Pattern
Burst	
Delay	Internal: 0 to 2147483640 bits, 8 bits step Ext Trigger, Enable: 0 to 2147483520 bits, 8 bits step Adjust Method: Auto, Manual
Enable Period	Internal: 12800 bits to 2147482624 bits, 256 bits step Ext Trigger: 12800 bits to 2147483392 bits, 256 bits step
Burst Cycle	25600 bits to 2147483648 bits, 1024 bits step

Measurement

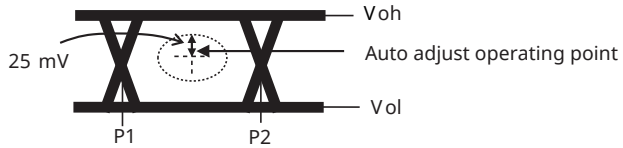
Measurement Types	Error Rate Error Count Error Interval %Error Free Interval Frequency Frequency measurement accuracy Clock Count Sync Loss Interval Clock Loss Interval
Error Detection Mode	• Total, Insertion, Omission • Transition, Non Transition
SKP OS Filtering	This function filters SKP OS in conformance with the USB3.1 Gen1/2 and PCIe 1/2/3/4/5 standards. Operation at each standard bit rate only is supported.

Error Analysis

Block Window	Excludes the specified data pattern bit from the measurement target according to the settings. (Mask measurement function) Invalid when "Mixed" pattern or "HSSB Data" is selected for Test Pattern.
Bit Window	Excludes any channels among internal 32 channels from the measurement target.
Capture Function	
Automatic Measurement Function	Eye margin*1, *2, Bathtub*1, *2, Eye Contour*1, *2, PAM4 BER measurement Auto Adjust*3, *4, *5, Auto Search*3, Auto Search PAM4 mode

*1: Not available when "HSSB Data" is selected for Test Pattern.
*2: Unavailable when the system clock is set to Clock and Data Recovery.
*3: The input pattern must be an NRZ PRBS pattern with a mark ratio of 1/2.
*4: The Auto Adjust function obtains a point in the vicinity of the following as an optimum point:
- (Voh + Vol)/2 in voltage direction
- (P1 + P2)/2 in phase direction

The Auto Adjust function works properly when there are no mask-hits which are observed by the oscilloscope vertically within ±25 mV area from the Auto Adjust operating point.



*5: If eye diagram of input signal is not symmetry, the Auto Adjust may not adjust input signals to the optimum value.
The Auto Search Fine is recommended to measure asymmetric input signals.

Variable Clock Delay

Phase Variable Range	–1000 mUI to +1000 mUI, 2 mUI step
Phase Setting Error	±50 m UIp-p (typ.)*
Calibration Indicator	This indicator is on when Calibration is required due to: • Change in 1/1Clock frequency by ±250 kHz. • Change in the ambient temperature by ±5°C.

*: Using oscilloscope with residual jitter of less than 200 fs rms

Clock Recovery

Clock Source Options	Clock Recovery, Clock and Data Recovery Clock*1
Operating Bit Rate	At NRZ 2.4 Gbit/s to 21.0 Gbit/s*2 2.4 Gbit/s to 32.1 Gbit/s*3 At PAM4 2.4 Gbaud to 21.0 Gbaud 2.4 Gbaud to 28.1 Gbaud*3 28.1100001 Gbaud to 32.1 Gbaud (BER 1.0E-7 typ.)*3
Setting Range	2.400000 Gbit/s to 21.000000 Gbit/s, 0.000001 Gbit/s step*2 2.400000 Gbit/s to 32.100000 Gbit/s, 0.000001 Gbit/s step*3
Maximum Number of Consecutive Zeros*4	72 bit (Zero Substitution 2^{15})
Lock Range*4	±200 ppm
Target Loop Band	Available options are $\frac{\text{Bit rate}}{1667}$ MHz, $\frac{\text{Bit rate}}{2578}$ MHz, Jitter Tolerance*5 and Variable. If the Variable option is selected, the following settings are available:

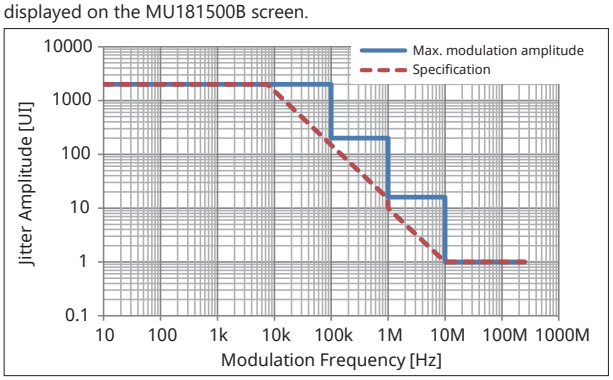
Bit Rate [Gbit/s]	Setting Range [MHz]	Step [MHz]
2.400000 to 5.500000	3	—
5.500001 to 7.500000	3 to 4	1
7.500001 to 9.500000	3 to 5	1
9.500001 to 10.500000	3 to 6	1
10.500001 to 12.500000	3 to 7	1
12.500001 to 14.500000	3 to 8	1
14.500001 to 15.500000	3 to 9	1
15.500001 to 17.500000	3 to 10	1
17.500001 to 19.500000	3 to 11	1
19.500001 to 20.500000	3 to 12	1
20.500001 to 22.500000	3 to 13	1
22.500001 to 24.500000	3 to 14	1
24.500001 to 25.500000	3 to 15	1
25.500001 to 27.500000	3 to 16	1
27.500001 to 29.500000	3 to 17	1
29.500001 to 30.500000	11 to 18	1
30.500001 to 32.100000	11 to 19	1

Jitter Tolerance	
Clock Recovery	At the bit rate of 28.05 Gbit/s, conforming to Jitter Tolerance Mask defined by the "32G FC standard" At the bit rate of 25.78125 Gbit/s, conforming to Jitter Tolerance Mask defined by the "100 GbE (25.78 × 4) standard" At the bit rate of 14.0625 Gbit/s, conforming to Jitter Tolerance Mask defined by the "InfiniBand FDR standard" At the bit rate of 14.025 Gbit/s, conforming to Jitter Tolerance Mask defined by the "16G FC standard" At the bit rate of 10.3125 Gbit/s, conforming to Jitter Tolerance Mask defined by the "10 GbE standard"

*1: Can be selected when option x22 installed. Clock Recovery from data input to Data1 Input. PRBS input pattern and 1/2 Mark Ratio at NRZ.
At PAM4, Clock Recovery at Middle Eye for Data1 with PRBS15, and Upper/Middle/Lower Eye for Data2.
*2: When option x22 is installed.
*3: When option x01 is installed.
*4: When the option x22 is installed:
The target loop band is specified by the maximum setting value of each bit rate.
*5: The Jitter Tolerance option makes the loop band wider than the other options and enables the Jitter Tolerance measurement.

Jitter Tolerance

Jitter Tolerance	
	Bit rate: 16 Gbit/s, 28.1 Gbit/s*, 32.1 Gbit/s* Pattern: PRBS $2^{31} - 1$ SSC with a 5300 ppm amplitude and RJ of 0.3 UI can be simultaneously applied by using MU181500B. These specifications are defined assuming the following conditions: Loopback connection to the MU195020A, defined by one specific temperature in the range of 20°C to 30°C. When RJ + BUJ is bigger than 0.5 UIp-p or SJ + RJ + BUJ is bigger than the standard value + 0.3 UIp-p, "Overload" is displayed on the MU181500B screen.



Modulation Frequency [Hz]	Max. Modulation Amplitude [UIp-p]	Specification [UIp-p]
10	2,000	2,000
7,500	2,000	2,000
100,000	2,000	150
1,000,000	200	15
10,000,000	16	1
250,000,000	1	1

*: Option x01 available

Multichannel Operation

Combination*1	
Number of Channels	2
Pattern	At Combination n = 2 below (2ch combination)
Data	Pattern Length 2 × n to 268435456 × n bits, n bits step*2
Mixed	Row Length 2048 × n to (268435456 + 2^{31}) × n bits, 1024 × n bits step*2 Pattern Length 1024 × n to 268435456 × n bits, n bits step*2

*1: Combination extending over multiple slots cannot be set. Cannot be set when Test Pattern is HSSB Data.
*2: Common to every channel specified by Combination Setting.

SI ED MU195040A Specifications

Automatic Measurement Function

Eye Contour	Measurement target Data 1 to Data n*1
Eye Margin	Measurement target Data 1 to Data n*1
Bathtub	Measurement target Data 1 to Data n*1
Capture	2Ch Combination is available*2
PAM4 BER Measurement	The following pattern selectable • GrayPRBS7, 9, 10, 11, 13Q-IEEE200G_400G [Draft2], 15,20 • GrayPrePRBS20 • GrayPreQPRBS13-CEI • GrayPreQPRBS13-IEEE100GBASE-KP4_Lane0, 1, 2, 3 • GrayPRQS10 • GrayQPRBS13-CEI • GrayQPRBS13-IEEE100GBASE-KP4_Lane0, 1, 2, 3 • GraySSPR • PRBS7, 9, 10, 11, 13Q-IEEE200G_400G [Draft2], 15, 20 • PrePRBS20 • PreQPRBS13-CEI • PRQS10 • QPRBS13-CEI • QPRBS13-IEEE100GBASE-KP4_Lane0, 1, 2, 3 • Squarewave • SSPR • SSPRQ • Transmitter_Linearity

*1: Separately specified for each channel.
*2: Common to every channel specified by Combination Setting.

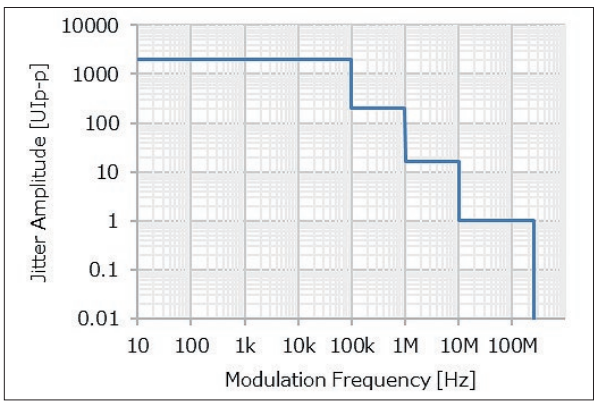
General (MU195020A/MU195040A)

Dimensions and Mass	234 (W) × 21 (H) × 175 (D) mm (Excluding protrusions), 2.5 kg max.
Operating Temperature	15°C to 35°C

Operating Baud Rate

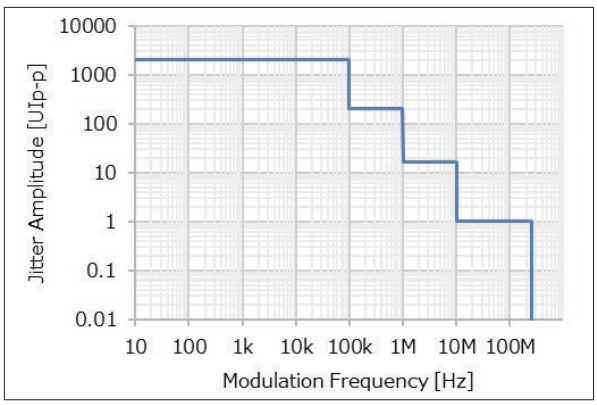
<table>
<tr><td>Operating Baud/Bit Rate</td><td>The setting range is the same for the baud rate of PAM4/PAM3 output and the bit rate of NRZ output. Only the baud rate setting range is described below.</td></tr>
<tr><td>Setting Range/Step</td><td>The baud rate setting range is determined by the upper limit baud rate options*1, *2, *3, the synchronized module (valid only when installed in the same chassis as the MU196020C), clock output frequency (Section 13.1), and applications*4.
Application:
When the Expert BERT application is selected: 2.4 to 32.1*1/58.2*2/64.2*3 Gbaud
When the BERT for PCIe1-7 application is selected: 2.4 to 64.2 Gbaud*4</td></tr>
<tr><td>Operating Baud Rate Setting Range (MU181000A/B synchronized operation)*5</td><td>2.400 000 to 25.000 000 Gbaud, 0.000 002 Gbaud step*1, *2, *3
25.000 004 to 32.100 000*1/50.000 000*2, *3 Gbaud, 0.000 004 Gbaud step
50.000 008 to 58.200 000*2/64.200 000*3 Gbaud, 0.000 008 Gbaud step</td></tr>
<tr><td>Operating Baud Rate Setting Range (MU181000A/B and MU181500B synchronized operation)*5</td><td>2.400 000 to 3.125 000 Gbaud, 0.000 002 Gbaud step
3.200 002 to 6.250 000 Gbaud, 0.000 002 Gbaud step
6.400 002 to 12.500 000 Gbaud, 0.000 002 Gbaud step
12.800 002 to 25.000 000 Gbaud, 0.000 002 Gbaud step
25.600 004 to 32.100 000*1/50.000 000*2 Gbaud, 0.000 004 Gbaud step
51.200 008 to 58.200 000*2/64.200 000*3 Gbaud, 0.000 008 Gbaud step</td></tr>
<tr><td>Operating Baud Rate Setting Range (MU191000A synchronized operation)*5</td><td>2.400 000 to 25.600 000 Gbaud, 0.000 002 Gbaud step*1, *2, *3
25.600 004 to 32.100 000*1/51.200 000*2, *3 Gbaud, 0.000 004 Gbaud step
51.200 008 to 58.200 000*2/64.200 000*2 Gbaud, 0.000 008 Gbaud step</td></tr>
<tr><td>Operating Baud Rate Setting Range (MU191000A/B and MU181500B synchronized operation)*5</td><td>2.400 000 to 25.600 000 Gbaud, 0.000 002 Gbaud step
25.600 004 to 32.100 000*1/51.200 000*2 Gbaud, 0.000 004 Gbaud step
51.200 008 to 58.200 000*2/64.200 000*3 Gbaud, 0.000 008 Gbaud step</td></tr>
<tr><td>Operating Baud Rate Setting Range (MU181500B synchronized operation with external clock source)</td><td>Clock Output Rate Full Rate
<table>
<tr><th>Baud Rate Setting Range</th><th>Input Clock Frequency</th><th>Relationship Between Baud Rate and Input Clock Frequency</th></tr>
<tr><td>2.4 to 15.0 Gbaud</td><td>2.4 GHz to 15.0 GHz</td><td>Operate at 1/1 clock</td></tr>
<tr><td>15.0 to 30.0 Gbaud</td><td>7.5 GHz to 15.0 GHz</td><td>Operate at 1/2 clock</td></tr>
<tr><td>25.0 to 32.1 Gbaud</td><td>6.25 GHz to 8.025 GHz</td><td>Operate at 1/4 clock</td></tr>
</table>
Clock Output Rate Half Rate, Quarter Rate
<table>
<tr><th>Baud Rate Setting Range</th><th>Input Clock Frequency</th><th>Relationship Between Baud Rate and Input Clock Frequency</th></tr>
<tr><td>2.4 to 30.0 Gbaud*1, *2, *3</td><td>1.2 GHz to 15.0 GHz</td><td>Operate at 1/2 clock</td></tr>
<tr><td>30.0 to 32.1*1, *4/58.2*2/ 60.0*3 Gbaud</td><td>7.5 GHz to 8.025*1,* 4/ 14.55*2/15.0*3 GHz</td><td>Operate at 1/4 clock</td></tr>
<tr><td>50.0 to 58.2*2/64.2*3 Gbaud</td><td>6.25 GHz to 7.275*2 to 8.025*3 GHz</td><td>Operate at 1/8 clock</td></tr>
</table></td></tr>
<tr><td>Operating Baud Rate Setting Range (With external clock source)</td><td>Clock Output Rate Full Rate
<table>
<tr><th>Baud Rate Setting Range</th><th>Input Clock Frequency</th><th>Relationship Between Baud Rate and Input Clock Frequency</th></tr>
<tr><td>2.4 to 16.05 Gbaud</td><td>2.4 GHz to 16.05 GHz</td><td>Operate at 1/1 clock</td></tr>
<tr><td>16.05 to 32.1 Gbaud</td><td>8.025 GHz to 16.05 GHz</td><td>Operate at 1/2 clock</td></tr>
<tr><td>25.0 to 32.1 Gbaud</td><td>6.25 GHz to 8.025 GHz</td><td>Operate at 1/4 clock</td></tr>
</table>
Clock Output Rate Half Rate, Quarter Rate
<table>
<tr><th>Baud Rate Setting Range</th><th>Input Clock Frequency</th><th>Relationship Between Baud Rate and Input Clock Frequency</th></tr>
<tr><td>2.4 to 30.0 Gbaud*1, *2, *3</td><td>1.2 GHz to 15.0 GHz</td><td>Operate at 1/2 clock</td></tr>
<tr><td>30.0 to 32.1*1, *4/58.2*2/ 60.0*3 Gbaud</td><td>7.5 GHz to 8.025*1,* 4/ 14.55*2/15.0*3 GHz</td><td>Operate at 1/4 clock</td></tr>
<tr><td>50.0 to 58.2*2/64.2*3 Gbaud</td><td>6.25 GHz to 7.275*2 to 8.025*3 GHz</td><td>Operate at 1/8 clock</td></tr>
</table></td></tr>
<tr><td>Offset Setting Range/Step</td><td>Available only when synchronized with the MU181000A/B or MU191000A.</td></tr>
<tr><td>MU181000A/B synchronized operation</td><td>–1000 to +1000 ppm, 1 ppm step
For the following bit rates, the setting range is –1000 to 0 ppm.
Clock Output Rate Full Rate 12.500 000 Gbaud, 25.000 000 Gbaud
Clock Output Rate Half Rate, Quarter Rate 25.000 000 Gbaud, 50.000 000 Gbaud</td></tr>
<tr><td>MU191000A synchronized operation</td><td>–1000 to +1000 ppm, 1 ppm step
For the following bit rates, the setting range is –1000 to 0 ppm.
Clock Output Rate Full Rate 12.800 000 Gbaud, 25.600 000 Gbaud
Clock Output Rate Half Rate, Quarter Rate 25.600 000 Gbaud, 51.200 000 Gbaud</td></tr>
</table>

Jitter Setting Range	When synchronized with the MU181000A/B + MU181500B or MU191000A + MU181500B
SJ1 Setting Range	When the SJ2 switch is the built-in SJ2, the jitter amplitude that can be set is reduced by half
SJ1 Clock Output Rate Full Rate Setting Range	30 < Baud rate ≤ 32.1 Gbaud, 15 < Baud rate ≤ 17 Gbaud



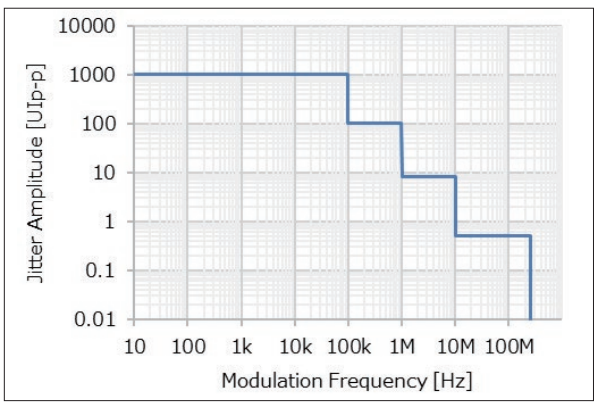
Modulation Frequency [Hz]	Jitter Amplitude [UIp-p]
10 to 100k	0 to 2000
100.1k to 1M	0 to 200
1.001M to 10M	0 to 16
10.01M to 150M	0 to 1

17 < Baud rate ≤ 30 Gbaud



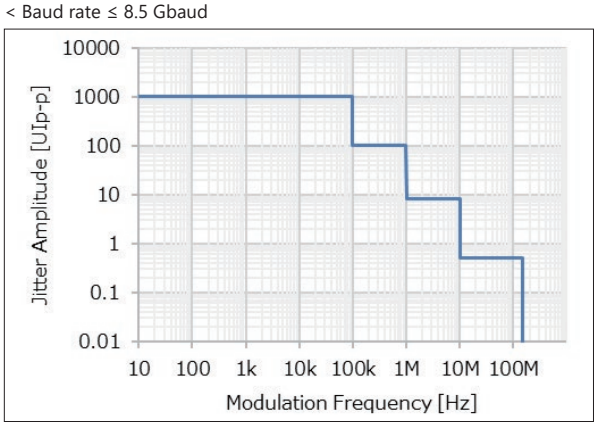
Modulation Frequency [Hz]	Jitter Amplitude [UIp-p]
10 to 100k	0 to 2000
100.1k to 1M	0 to 200
1.001M to 10M	0 to 16
10.01M to 250M	0 to 1

8.5 < Baud rate ≤ 15 Gbaud



Modulation Frequency [Hz]	Jitter Amplitude [UIp-p]
10 to 100k	0 to 1000
100.1k to 1M	0 to 100
1.001M to 10M	0 to 8
10.01M to 250M	0 to 0.5

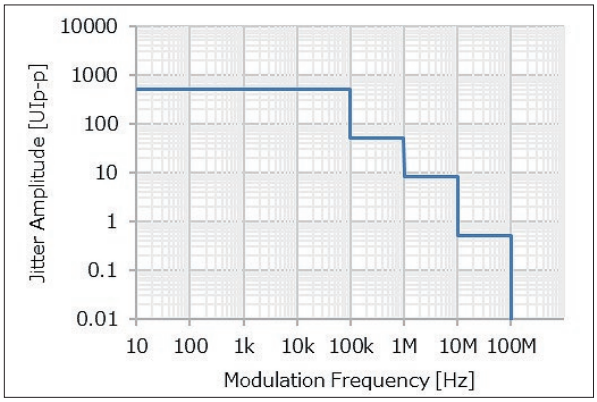
4 < Baud rate ≤ 8.5 Gbaud



Modulation Frequency [Hz]	Jitter Amplitude [UIp-p]
10 to 100k	0 to 1000
100.1k to 1M	0 to 100
1.001M to 10M	0 to 8
10.01M to 150M	0 to 0.5

SJ1
Clock Output Rate
Full Rate Setting Range

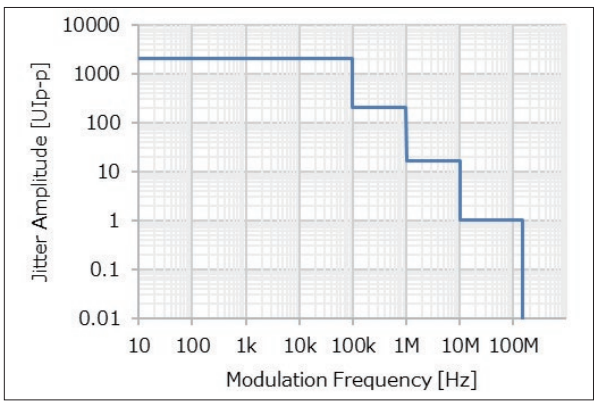
2.4 ≤ Baud rate ≤ 4 Gbaud



Modulation Frequency [Hz]	Jitter Amplitude [UIp-p]
10 to 100k	0 to 500
100.1k to 1M	0 to 50
1.001M to 10M	0 to 8
10.01M to 100M	0 to 0.5

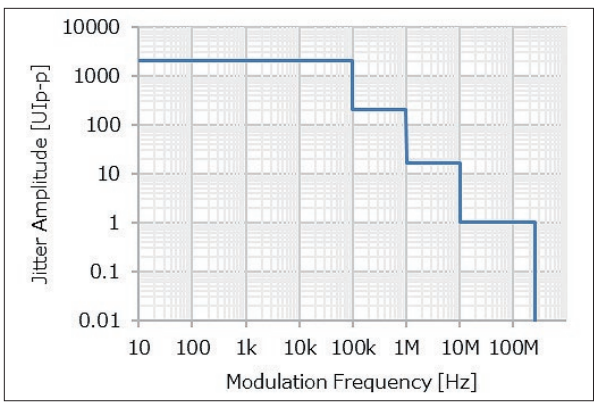
SJ1
Clock Output Rate
Half Rate, Quarter Rate
Setting Range

60 < Baud rate ≤ 64.2 Gbaud, 30 < Baud rate ≤ 34 Gbaud, 8 < Baud rate ≤ 17 Gbaud



Modulation Frequency [Hz]	Jitter Amplitude [UIp-p]
10 to 100k	0 to 2000
100.1k to 1M	0 to 200
1.001M to 10M	0 to 16
10.01M to 150M	0 to 1

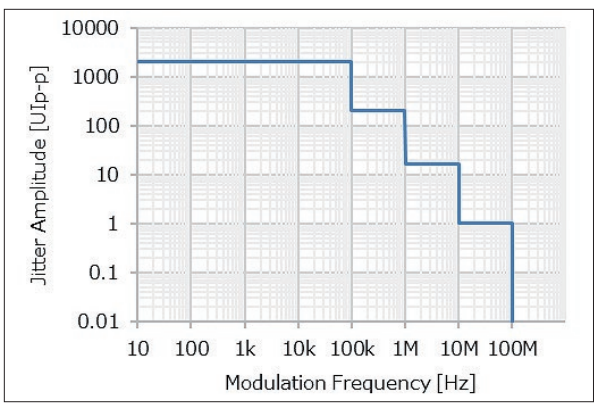
34 < Baud rate ≤ 60 Gbaud*, 17 < Baud rate ≤ 30 Gbaud



Modulation Frequency [Hz]	Jitter Amplitude [UIp-p]
10 to 100k	0 to 2000
100.1k to 1M	0 to 200
1.001M to 10M	0 to 16
10.01M to 250M*	0 to 1

* When the operation baud rate is equal to or more than 50 Gbaud and equal to or less than 60 Gbaud and the relation between baud rate and input clock frequency in 3.1.3.2 Clock Output Rate Half Rate and Quarter Rate is set to 1/8 Clock Input, Fm [Hz] is 10.01 to 150 MHz.

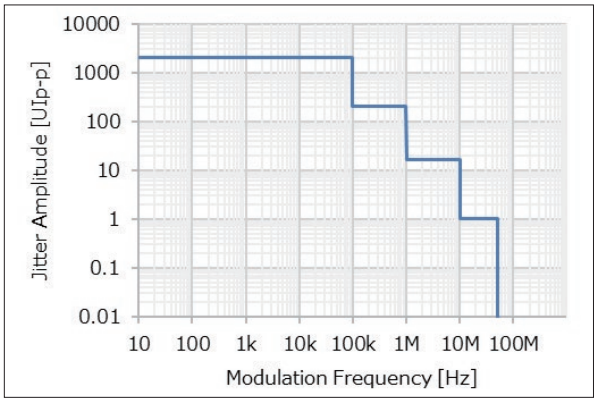
2.4 < Baud rate ≤ 8 Gbaud



Modulation Frequency [Hz]	Jitter Amplitude [UIp-p]
10 to 100k	0 to 2000
100.1k to 1M	0 to 200
1.001M to 10M	0 to 16
10.01M to 100M	0 to 1

SJ1
Clock Output Rate
Half Rate, Quarter Rate
Setting Range

Baud rate 2.4 Gbaud



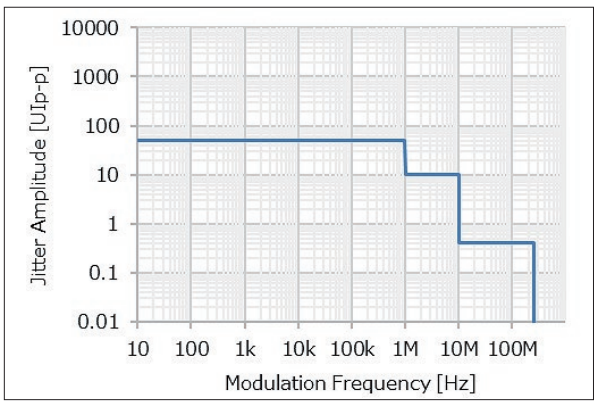
Modulation Frequency [Hz]	Jitter Amplitude [UIp-p]
10 to 100k	0 to 2000
100.1k to 1M	0 to 200
1.001M to 10M	0 to 16
10.01M to 50M	0 to 1

SJ2 Setting Range

When synchronized with the MU181000A/B + MU181500B or MU191000A + MU181500B
Either SJ2 via MU181000A/B Clock*6 or Built-in SJ2 can be selected.

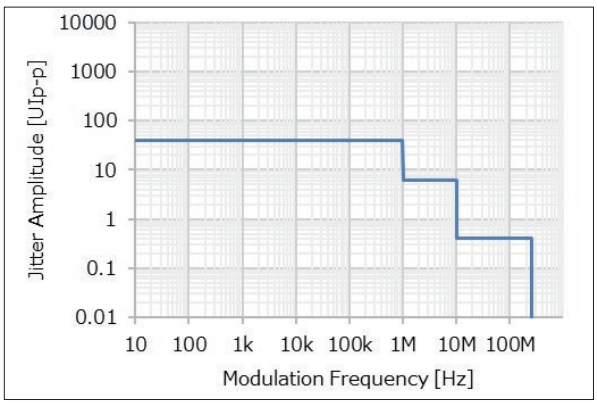
SJ2
via MU181000A/B
Clock Output Rate
Full Rate Setting Range*6

15.000 001 ≤ Baud rate ≤ 32.1 Gbaud



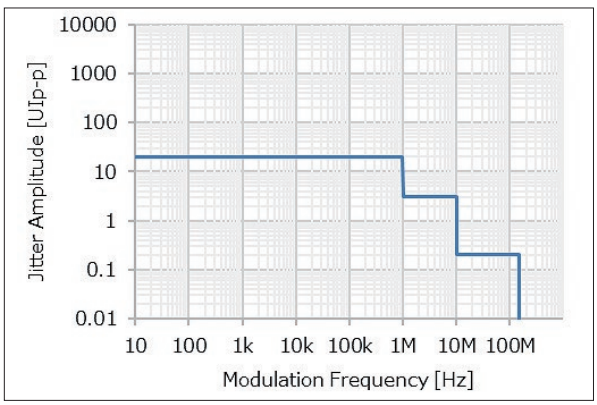
Modulation Frequency [Hz]	Jitter Amplitude [UIp-p]
10 to 1M	0 to 50
1.001M to 10M	0 to 10
10.01M to 250M	0 to 0.4

6.400 001 ≤ Baud rate ≤ 15 Gbaud



Modulation Frequency [Hz]	Jitter Amplitude [UIp-p]
10 to 1M	0 to 40
1.001M to 10M	0 to 6
10.01M to 250M	0 to 0.4

3.200 001 ≤ Baud rate ≤ 6.25 Gbaud

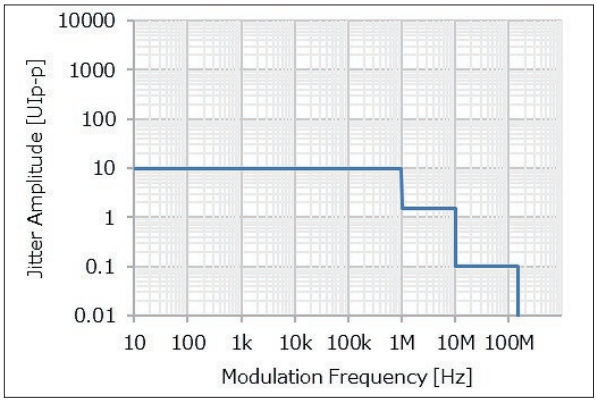


Modulation Frequency [Hz]	Jitter Amplitude [UIp-p]
10 to 1M	0 to 20
1.001M to 10M	0 to 3
10.01M to 150M	0 to 0.2

PAM4 PPG MU196020C Specifications

SJ2
via MU181000A/B
Clock Output Rate
Full Rate Setting Range*6

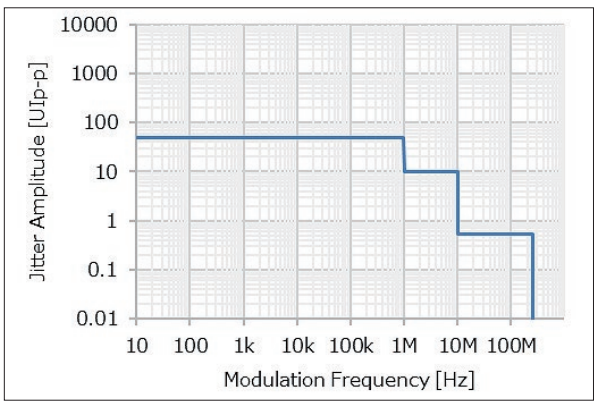
2.4 ≤ Baud rate ≤ 3.125 Gbaud



Modulation Frequency [Hz]	Jitter Amplitude [UIp-p]
10 to 1M	0 to 10
1.001M to 10M	0 to 1.5
10.01M to 150M	0 to 0.1

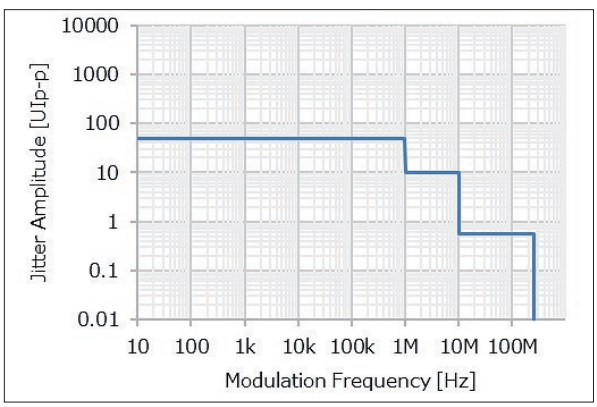
SJ2
via MU181000A/B
Clock Output Rate
Half Rate, Quarter Rate
Setting Range*6

60.000 001 ≤ Baud rate ≤ 64.2 Gbaud



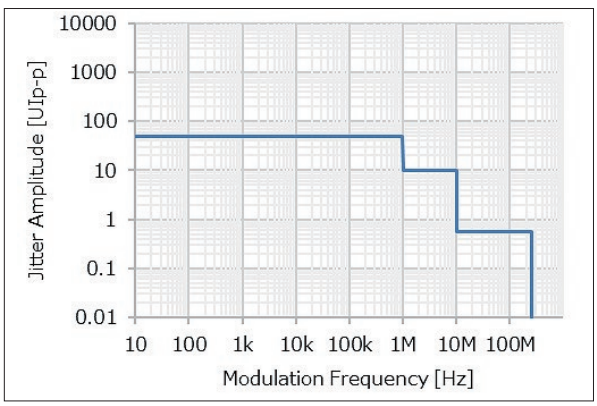
Modulation Frequency [Hz]	Jitter Amplitude [UIp-p]
10 to 1M	0 to 50
1.001M to 10M	0 to 10
10.01M to 250M	0 to 0.544

30.000 001 ≤ Baud rate ≤ 60.0 Gbaud



Modulation Frequency [Hz]	Jitter Amplitude [UIp-p]
10 to 1M	0 to 50
1.001M to 10M	0 to 10
10.01M to 250M	0 to 0.548

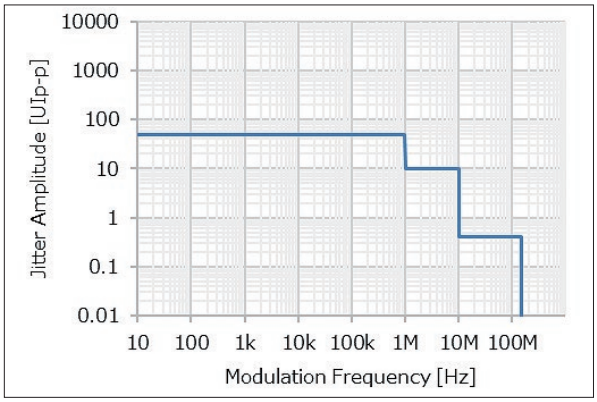
12.800001 ≤ Baud rate ≤ 30.0 Gbaud



Modulation Frequency [Hz]	Jitter Amplitude [UIp-p]
10 to 1M	0 to 50
1.001M to 10M	0 to 10
10.01M to 250M	0 to 0.55

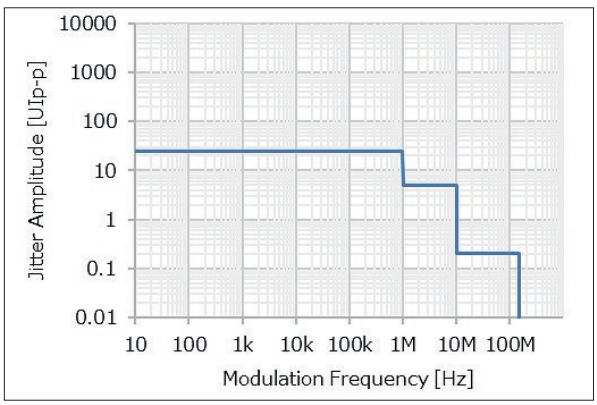
SJ2
via MU181000A/B
Clock Output Rate
Half Rate, Quarter Rate
Setting Range*6

6.400001 ≤ Baud rate ≤ 12.5 Gbaud



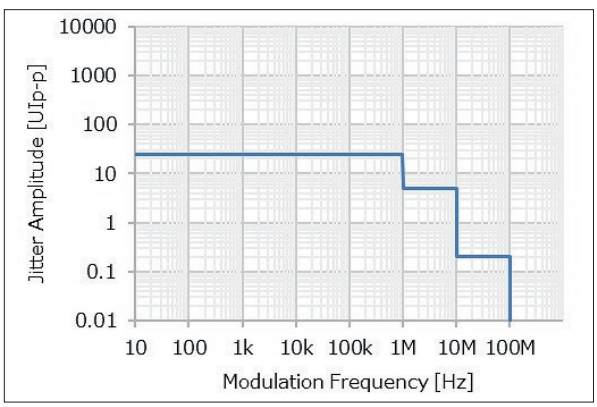
Modulation Frequency [Hz]	Jitter Amplitude [UIp-p]
10 to 1M	0 to 50
1.001M to 10M	0 to 10
10.01M to 150M	0 to 0.4

3.600001 ≤ Baud rate ≤ 6.25 Gbaud



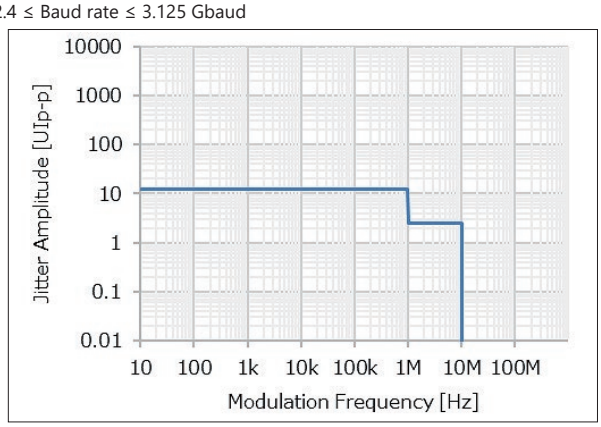
Modulation Frequency [Hz]	Jitter Amplitude [UIp-p]
10 to 1M	0 to 25
1.001M to 10M	0 to 5
10.01M to 150M	0 to 0.2

3.200001 < Baud rate ≤ 3.6 Gbaud



Modulation Frequency [Hz]	Jitter Amplitude [UIp-p]
10 to 1M	0 to 25
1.001M to 10M	0 to 5
10.01M to 100M	0 to 0.2

2.4 ≤ Baud rate ≤ 3.125 Gbaud



Modulation Frequency [Hz]	Jitter Amplitude [UIp-p]
10 to 1M	0 to 12.4
1.001M to 10M	0 to 2.5

<table>
<tr>
<td>Built-in SJ2 Clock Output Rate Full Rate Setting Range</td>
<td>
15 < Baud rate ≤ 32.1 Gbaud
<table>
<tr><th>Modulation Frequency [Hz]</th><th>Jitter Amplitude [UIp-p]</th></tr>
<tr><td>33k</td><td>0 to 1000</td></tr>
<tr><td>87M</td><td>0 to 0.5</td></tr>
<tr><td>100M</td><td>0 to 0.5</td></tr>
<tr><td>210M</td><td>0 to 0.2</td></tr>
</table>
4 < Baud rate ≤ 15 Gbaud
<table>
<tr><th>Modulation Frequency [Hz]</th><th>Jitter Amplitude [UIp-p]</th></tr>
<tr><td>33k</td><td>0 to 500</td></tr>
<tr><td>87M</td><td>0 to 0.25</td></tr>
<tr><td>100M</td><td>0 to 0.25</td></tr>
<tr><td>210M</td><td>0 to 0.1</td></tr>
</table>
2.4 ≤ Baud rate ≤ 4 Gbaud
<table>
<tr><th>Modulation Frequency [Hz]</th><th>Jitter Amplitude [UIp-p]</th></tr>
<tr><td>33k</td><td>0 to 500</td></tr>
<tr><td>87M</td><td>0 to 0.25</td></tr>
<tr><td>100M</td><td>0 to 0.25</td></tr>
</table>
</td>
</tr>
<tr>
<td>Built-in SJ2 Clock Output Rate Half Rate, Quarter Rate Setting Range</td>
<td>
8 < Baud rate ≤ 64.2 Gbaud
<table>
<tr><th>Modulation Frequency [Hz]</th><th>Jitter Amplitude [UIp-p]</th></tr>
<tr><td>33k</td><td>0 to 1000</td></tr>
<tr><td>87M</td><td>0 to 0.5</td></tr>
<tr><td>100M</td><td>0 to 0.5</td></tr>
<tr><td>210M</td><td>0 to 0.2</td></tr>
</table>
2.4 < Baud rate ≤ 8 Gbaud
<table>
<tr><th>Modulation Frequency [Hz]</th><th>Jitter Amplitude [UIp-p]</th></tr>
<tr><td>33k</td><td>0 to 1000</td></tr>
<tr><td>87M</td><td>0 to 0.5</td></tr>
<tr><td>100M</td><td>0 to 0.5</td></tr>
</table>
Baud rate 2.4 Gbaud
<table>
<tr><th>Modulation Frequency [Hz]</th><th>Jitter Amplitude [UIp-p]</th></tr>
<tr><td>33k</td><td>0 to 1000</td></tr>
</table>
</td>
</tr>
</table>

*1: When the Option 001 is installed.
*2: When the Option 002 or 112 is installed.
*3: When the Option 003, 113, or 123 is installed.
*4: When the BERT for PCIe1-7 application is selected.
*5: Synchronization not allowed when Unit Sync is ON.
*6: Only when synchronized with MU181000A/B + MU181500B.

PAM4 PPG MU196020C Specifications

External Clock Input

Number of Input	1 (Single-end)
Input Frequency Range	1.2 GHz to 16.05 GHz
Input Amplitude	0.3 Vp-p to 1.0 Vp-p (–6.5 to +4.0 dBm)
Termination	50Ω, AC Coupling
Connector	SMA (J)

Aux Input

Number of Input	1 (Single-end)
Variation	Error Injection, Burst, Unit Sync, Jitter Sync
Minimum Pulse Width	1/256 of data rate
Input level	0/–1V (H: –0.25 V to 0.05 V, L: –1.1 V to –0.8 V) 0/–0.5 V (H: –0.05 V to 0.05 V, L: –0.55 V to –0.45 V) Vth 0 V (Input amplitude: 0.5 Vp-p to 1.0 Vp-p) Select one of the above.
Termination	GND, 50Ω
Connector	SMA (J)

Aux Output

Number of Output	2 (Differential)
Output Control	ON/OFF switching
Variation	1/n Clock (n = 8, 12, 16, 20 ... 1020, 1024), Pattern Sync, Burst Out2
Pattern Sync	PRBS, PRGM Position: 1 to {(Least common multiple of Pattern Length' and 256) –263}, in 8 steps When the pattern length is 1023 bits or less, Pattern Length' is the length as an integer multiple so that it becomes 1024 bits or more.
Burst Out2	Burst Trigger Delay: 0 to (Burst Cycle – 256) bits, 8 bits step Pulse Width: 16 bits to (Burst Cycle – 256) bits, 8 bits step
Output Level	0/–0.6 V (H: –0.25 V to 0.05 V, L: –0.80 V to –0.45 V)
Termination	GND, 50Ω
Connector	SMA (J)

Gating Output

Number of Output	1 (Single-end)
Output Control	ON/OFF switching
Variation	Burst, Repeat
Burst	Burst Output
Burst Trigger Delay	0 to (Burst Cycle – 256) bits, 8 bits step
Enable Pulse Width	16 bits to (Burst Cycle – 256) bits, 8 bits step
Repeat	Timing Signal Output
Timing Signal Cycle	$\mathrm{INT}\left(\frac{\text{Pattern length'}}{256}\right) \times 256$
Timing Signal Delay	0 to {(Least common multiple of Pattern Length' and 256) –256} The maximum settable number is 68 719 476 480, in 8- bit steps. When the pattern length is 1023 bits or less, Pattern Length' is the length as an integer multiple so that it becomes 1024 bits or more.
Timing Signal Pulse Width	256 to {(Least common multiple of Pattern Length' and 256) –256} The maximum settable number is 68 719 476 480, in 8- bit steps. When the pattern length is 1023 bits or less, Pattern Length' is the length as an integer multiple so that it becomes 1024 bits or more.
Unit Sync Output	
Output Level	0/–1 V (H: –0.25 V to 0.05 V, L: –1.25 V to –0.8 V) *
Termination	GND, 50Ω
Connector	SMA (f)

*: L: Output Enable, H: Output Disable

Generated Pattern*1

PRBS	
Pattern Length	$2^n - 1$ (n = 7, 9, 10, 11, 13, 15, 20, 23, 31)
Mark Ratio	1/2 (1/2INV is supported by a logical inversion.)
PRBS Generator Polynomial	n = 7: $1 + X^6 + X^7$ n = 9: $1 + X^5 + X^9$ n = 10: $1 + X^7 + X^{10}$ n = 11: $1 + X^9 + X^{11}$ n = 13: $1 + X + X^2 + X^{12} + X^{13}$ n = 15: $1 + X^{14} + X^{15}$ n = 20: $1 + X^3 + X^{20}$ n = 23: $1 + X^{18} + X^{23}$ n = 31: $1 + X^{28} + X^{31}$
PRBS Inversion	This is available in PAM4 mode only. Logical inversion of PRBS can be set independently for MSB and LSB.
PRBS 1st Bit	This can be selected when the first bit of the PRBS Generator is selected as the MSB or LSB.
Zero-Substitution	This is available in NRZ mode only.
Additional Bit	0 bit, 1 bit
Pattern Length	2^n or $2^n - 1$ (n = 7, 9, 10, 11, 15, 20, 23)
Start Position	Substitutes the bit coming after the maximum "0" successive bits.
Length of Consecutive Zero Bits	1 bits to (Pattern Length – 1) bits If the bit coming after Zero-substitution is "0", then it is replaced with "1".
Data	
Data Length	NRZ: 2 bits to 268 435 456 bits, 1 bit step PAM4/PAM3: 2 to 268 435 456 symbols, 1 symbol step
Bit Shift	This is available in PAM4 mode only. Bit shift of MSBs can be controlled in the range of ±256 bits (in 1-bit steps).
Standard Pattern (PAM4)	Standard-compliant PAM4-mode patterns
CEI	QPRBS13-CEI, QPRBS31-CEI
IEEE	IEEE802.3bs/cd: PRBS13Q, PRBS31Q, SSPRQ, Square Wave IEEE802.3bj: QPRBS13, JP03A, JP03B, Transmitter Linearity
InfiniBand	PRBS13Q (InfiniBand), PRBS23Q, PRBS31Q (InfiniBand)
Fibre Channel	PRBS31Q (Fibre Channel)
RS-FEC (Option 042)	RS-FEC Scrambled Idle 50G 1 Lane RS-FEC Scrambled Idle 100G 1 Lane (53.125 Gbaud, 100GBASE-DR/KR1/CR1) RS-FEC-Int Scrambled Idle 100G 1 Lane (53.125 Gbaud, 100GBASE-P) RS-FEC Scrambled Idle 100G 2 Lanes (26.5625 Gbaud, 100GBASE-KR2/CR2/SR2) RS-FEC Scrambled Idle 200G 4 Lanes (26.5625 Gbaud, 200GBASE-SR4/DR4/FR4/LR4) RS-FEC Scrambled Idle 200G 2 Lanes (53.125 Gbaud, 200GBASE-KR2/CR2) RS-FEC Scrambled Idle 400G 4 Lanes (53.125 Gbaud, 400GBASE-DR4/KR4/CR4) RS-FEC Scrambled Idle 400G 8 Lanes (26.5625 Gbaud, 400GBASE-FR8/LR8)
PCIe	CP in 1b/1b Encoding for PCIe6 MCP in 1b/1b Encoding for PCIe6 Jitter Measurement Pattern in 1b/1b Encoding for PCIe6 High Swing Toggle Pattern in 1b/1b Encoding for PCIe6 Low Swing Toggle Pattern 1b/1b Encoding for PCIe6 Jitter Calibration Pattern for PCIe6 Preset Calibration Pattern for PCIe6 CP in 1b/1b Encoding for PCIe7 MCP in 1b/1b Encoding for PCIe7 Jitter Measurement Pattern in 1b/1b Encoding for PCIe7 High Swing Toggle Pattern in 1b/1b Encoding for PCIe7 Low Swing Toggle Pattern 1b/1b Encoding for PCIe7 Jitter Calibration Pattern for PCIe7 Preset Calibration Pattern for PCIe7 Option 043 NOP Flit Layout in a ×1 Link NOP Flit Layout in a ×2 Link NOP Flit Layout in a ×4 Link NOP Flit Layout in a ×8 Link NOP Flit Layout in a ×16 Link

Standard Pattern (NRZ)	
CEI	SSPR
RS-FEC (Option 042)	RS-FEC Scrambled Idle 25G 1Lane, RS-FEC Scrambled Idle 50G 2Lanes RS (544, 514), RS-FEC Scrambled Idle 100G 4Lanes, RS-FEC Scrambled Idle 100G 4Lanes RS (544, 514)
PCIe	CP in 8b/10b Encoding for PCIe1 MCP in 8b/10b Encoding for PCIe1 Jitter Calibration Pattern for PCIe1 Preset Calibration Pattern for PCIe1 CP in 8b/10b Encoding for PCIe2 MCP in 8b/10b Encoding for PCIe2 Jitter Calibration Pattern for PCIe2 Preset Calibration Pattern for PCIe2 CP in 128b/130b Encoding for PCIe3 MCP in 128b/130b Encoding for PCIe3 Jitter Calibration Pattern for PCIe3 Preset Calibration Pattern for PCIe3 CP in 128b/130b Encoding for PCIe4 MCP in 128b/130b Encoding for PCIe4 Jitter Calibration Pattern for PCIe4 Preset Calibration Pattern for PCIe4 CP in 128b/130b Encoding for PCIe5 MCP in 128b/130b Encoding for PCIe5 Jitter Calibration Pattern for PCIe5 Preset Calibration Pattern for PCIe5
PRTS	
PRTS Length	$3^n - 1$ (n = 7, 19)
PRTS generator polynomial	n = 7 : $1 + X^2 + 2X^7$ Over GF (3) n = 19 : $1 + X^2 + 2X^{19}$ Over GF (3)
PAM3 Standard Pattern (Option 045)	
USB4 Gen4	PRBS, TS2.clksw USB4 Gen4 Power Management State Signal USB4 Gen4 Rx Frequency Variation Training Sequence
USB4 Gen4 Power Management State Signal	tPeriod: 20 to 80 ns/10 ns step Duty Cycle: 45, 50, 55% tPreData: 80 to 120 ns/10 ns step LFPS Diff. Amp.: Displays LFPS differential amplitude. LFPS Repetition: 50 to 150 times/10 times step USB4 Data: $PRBS^n$ (n = 7, 9, 10, 11, 13, 15, 20, 23, 31) PRTS7, 19 Data TS2.clksw Transmit: Starts LFPS signal transmission. Manual: Initiates a state transition from LFPS signal to USB4 Data. Break: Manual/Auto selection When Manual is selected, pressing the Manual button initiates a transition to the next state. When Auto is selected, a transition to the next state occurs at a specified timing. LFPS Swing: High/Low LFPS amplitude setting High: Output at the 0/2 Level amplitude, Low: Output at the 0/1 Level amplitude
USB4 Gen4 Rx Frequency Variation Training Sequence	Synchronized with the SSC clock switching function of MU181500B. Transmit: Starts the Rx Frequency Variation Training Sequence signal. Manual: Changes the output pattern. Time: Sets the output time for each pattern. Pattern output time for other than the final state: 10.0 to 20.0 us/0.1 us step Pattern output time for the final state: 1 to 10,000 ms/1 ms step Pattern: Sets the sequence pattern. $PRBS^n$ (n = 7, 9, 10, 11, 13, 15, 20, 23, 31) PRTS7, 19 TS2.clksw Break: Manual/Auto selection When Manual is selected, pressing the Manual button initiates a transition to the next state. When Auto is selected, a transition to the next state occurs at a specified timing.

Pattern Sequence

Sequence	Repeat, Burst
Repeat	Continuous Pattern
Burst	This is available only when Coding is NRZ.
Source	Internal, External-Trigger (Aux Input), External-Enable (Aux Input)
Data Sequence	Restart, Consecutive, Continuous
Enable Period	Internal: 12,800 bits to 2,147,483,136 bits, 256 bits step Ext Trigger/Enable: 12,800 bits to 2,147,483,648 bits, 256 bits step
Burst Cycle	25,600 bits to 2,147,483,648 bits, 1,024 bits step

PAM4 PPG MU196020C Specifications

Coding

Coding	NRZ, PAM4, PAM3
NRZ	Normal, Invert
PAM4 Gray Coding	ON, OFF
PAM4 Precoding (1/ (1 + D) mod 4)*1	ON, OFF
Delay Symbol	ON, OFF
SKP	No SKP, SKP×1, SKP×2
Preset	P0, P1, P2, P3, P4, P5, P6, P7, P8, P9, P10
SRIS	ON, OFF
EIEOS	ON
PAM3 Precoding (1/ (1 + D) mod 3)*2	ON/OFF
Polarity Inverse	ON/OFF PAM3 signal polarity inversion

*1: Generator polynomial compliant with the IEEE802.3
*2: Generator polynomial compliant with USB4

Error Addition

Type	Bit, Error on MSB, Error on LSB, Error on LSB&MSB, RS-FEC Symbol Error (Option 042), PCIe6 FEC Symbol Error (Option 043)
Bit	This is available only when Coding is NRZ.
Source	Internal, External-Trigger (Rise edge trigger), External-Disable (L: Disable)
Error Variation	Repeat, Single, (Cannot be selected when Source is External-Trigger.)
Error Rate	*E – n (* = 1 to 9, n = 3 to 12), Upper limit is 3.0E–3 Error Route: Select 1 to 32, Scan
Bit/Burst	Bit and burst selection Burst Length: 1 to 256/1 Step
RS-FEC Symbol Error	Inserts error to change only one PAM4 signal level (Option 042) For PAM4, an error is inserted so that the PAM4 signal changes only by one level. NRZ: Inserts error at 10-bit gap PAM4: Inserts error at 10 PAM4 Symbol or 20 PAM4 Symbol gap
Source	Internal, External-Trigger (Rise edge trigger), External-Disable (L: Disable)
Error Variation	Repeat, Single (Cannot be selected when Source is External-Trigger.)
Symbol error per code word	When 1 to 20 coding is NRZ When 1 to 20 coding is PAM4
Total BER for All Lane	*E – n (* = 1 to 9, n = 3 to 12), Upper limit is 6.0E–3 Error addition range changes with number of Symbol Error per Codeword
BER for One Lane SER for One Lane	*E – n (* = 1 to 9, n = 3 to 12), Upper limit is 6.0E–3 Error addition range changes with number of Symbol Error per Codeword
Error Addition Method	Type1: Level 0 → Level 1, Level 1 → Level 2, Level 2 → Level 3, Level 3 → Level 2 Type2: Level 0 → Level 1, Level 1 → Level 2, Level 2 → Level 1, Level 3 → Level 2 Type3: Level 0 → Level 1, Level 1 → Level 0, Level 2 → Level 1, Level 3 → Level 2 Type4: Level 0 → Level 1, Level 1 → Level 0 or Level2, Level 2 → Level 1 or Level 3, Level 3 → Level 2 MSB Only: Level 0 → Level 2, Level 1 → Level 3, Level 2 → Level 0, Level 3 → Level 1 LSB Only: Level 0 → Level 1, Level 1 → Level 0, Level 2 → Level 3, Level 3 → Level 2 MSB or LSB: Level 0 → Level 1 or Level 2, Level 1 → Level 0 or Level 3, Level 2 → Level 0 or Level 3, Level 3 → Level 1 or Level 2 MSB and LSB: Level 0 → Level 3, Level 1 → Level 2, Level 2 → Level 1, Level 3 → Level 0 Valid only when coding is PAM4.
FEC Standard	When coding is NRZ RS-FEC Scrambled Idle 25G 1Lane, RS-FEC Scrambled Idle 50G 2Lanes RS (544,514), RS-FEC Scrambled Idle 100G 4Lanes, RS-FEC Scrambled Idle 100G 4Lanes RS (544,514) When coding is PAM4 RS-FEC Scrambled Idle 50G 1Lane, RS-FEC Scrambled Idle 100G 1Lane, RS-FEC-Int Scrambled Idle 100G 1Lane, RS-FEC Scrambled Idle 100G 2Lanes, RS-FEC Scrambled Idle 200G 2Lanes, RS-FEC Scrambled Idle 200G 4Lanes, RS-FEC Scrambled Idle 400G 4Lanes, RS-FEC Scrambled Idle 400G 8Lanes

Error on MSB	Adds the specified symbol error. This is available only when Coding is PAM4. The set error is added to MSB only.
Source	Internal, External-Trigger (Rise edge trigger), External-Disable (L: Disable)
Error Variation	Repeat, Single (Cannot be selected when Source is External-Trigger.)
Symbol Error Rate	*E – n (* = 1 to 9, n = 3 to 12), Upper limit is 3.0E–3
Symbol/Burst	Symbol, Burst Burst Length: 1 to 256/1 Step
Error on LSB	Adds the specified symbol error. This is available only when Coding is PAM4. The set error is added to LSB only.
Source	Internal, External-Trigger (Rise edge trigger), External-Disable (L: Disable)
Error Variation	Repeat, Single (Cannot be selected when Source is External-Trigger.)
Symbol Error Rate	*E – n (* = 1 to 9, n = 3 to 12), Upper limit is 3.0E–3
Symbol/Burst	Symbol, Burst Burst Length: 1 to 256/1 Step
Error on LSB&MSB	Adds the specified symbol error. This is available only when Coding is PAM4. An error is inserted to make the PAM4 signal change by one level only.
Source	Internal, External-Trigger (Rise edge trigger), External-Disable (L: Disable)
Error Variation	Repeat, Single (Cannot be selected when Source is External-Trigger.)
Symbol Error Rate	*E – n (* = 1 to 9, n = 3 to 12), Upper limit is 3.0E–3
Symbol/Burst	Symbol, Burst Burst Length: 1 to 256/1 Step
Error Addition Method	Type1: Level 0 → Level 1, Level 1 → Level 2, Level 2 → Level 3, Level 3 → Level 2 Type2: Level 0 → Level 1, Level 1 → Level 2, Level 2 → Level 1, Level 3 → Level 2 Type3: Level 0 → Level 1, Level 1 → Level 0, Level 2 → Level 1, Level 3 → Level 2 Type4: Level 0 → Level 1, Level 1 → Level 0 or Level2, Level 2 → Level 1 or Level 3, Level 3 → Level 2 MSB Only: Level 0 → Level 2, Level 1 → Level 3, Level 2 → Level 0, Level 3 → Level 1 LSB Only: Level 0 → Level 1, Level 1 → Level 0, Level 2 → Level 3, Level 3 → Level 2 MSB or LSB: Level 0 → Level 1 or Level 2, Level 1 → Level 0 or Level 3, Level 2 → Level 0 or Level 3, Level 3 → Level 1 or Level 2 MSB and LSB: Level 0 → Level 3, Level 1 → Level 2, Level 2 → Level 1, Level 3 → Level 0
PCIe6 FEC Symbol Error	Inserts error to change only one PAM4 signal level NRZ: Inserts error at 10-bit gap PAM4: Inserts error at 10 PAM4 Symbol or 20 PAM4 Symbol gap
Source	Internal, External-Trigger (Rise edge trigger), External-Disable (L: Disable)
Error Variation	Repeat, Single (Cannot be selected when Source is External-Trigger.)
PCIe6 Standard	x1 Link Common CLK/SRNS Mode x2 Link Common CLK/SRNS Mode x4 Link Common CLK/SRNS Mode x8 Link Common CLK/SRNS Mode x16 Link Common CLK/SRNS Mode x1 Link SRIS Mode x2 Link SRIS Mode x4 Link SRIS Mode x8 Link SRIS Mode x16 Link SRIS Mode
SKP	No SKP, SKPx1, SKPx2
Flit Error Interval	Add every 8 Bits (Do not distinguish ECC groups) Add every 24 Bits (Add to only one ECC group)
PAM4 Symbol Error per Flit	1 to 8 FEC Symbols, 1 FEC Symbol step If PCIe6 Standard is as follows, the upper limit is restricted to "4". [x16 Link Common CLK/SRNS Mode] [x16 Link SRIS Mode]
Flit Error per Control SKP Interval	1 to 4 Flits, 1 Flit step
Total BER for All Lane	*E – n (* = 1 to 9, n = 3 to 12), Upper limit is 7E–3 The error addition range changes with the values of PCIe6 Standard, PAM4 Symbol Error per Flit, and Flit Error per Control SKP Interval.
PAM4 Symbol Error for One Lane	*E – n (* = 1 to 9, n = 3 to 12), Upper limit is 7E–3 The error addition range changes with the values of PCIe6 Standard, PAM4 Symbol Error per Flit, and Flit Error per Control SKP Interval.

Error Addition Method	Type1: Level 0 → Level 1, Level 1 → Level 2, Level 2 → Level 3, Level 3 → Level 2 Type2: Level 0 → Level 1, Level 1 → Level 2, Level 2 → Level 1, Level 3 → Level 2 Type3: Level 0 → Level 1, Level 1 → Level 0, Level 2 → Level 1, Level 3 → Level 2 Type4: Level 0 → Level 1, Level 1 → Level 0 or Level2, Level 2 → Level 1 or Level 3, Level 3 → Level 2 MSB Only: Level 0 → Level 2, Level 1 → Level 3, Level 2 → Level 0, Level 3 → Level 1 LSB Only: Level 0 → Level 1, Level 1 → Level 0, Level 2 → Level 3, Level 3 → Level 2 MSB or LSB: Level 0 → Level 1 or Level 2, Level 1 → Level 0 or Level 3, Level 2 → Level 0 or Level 3, Level 3 → Level 1 or Level 2 MSB and LSB: Level 0 → Level 3, Level 1 → Level 2, Level 2 → Level 1, Level 3 → Level 0
PAM3 Error Addition	This is available when Coding is PAM3.
Error on LSB&MSB	Adds the specified symbol error.
Source	Internal, External-Trigger (Rise edge trigger), External-Disable (L: Disable)
Error Variation	Repeat, Single (Cannot be selected when Source is External-Trigger.)
Symbol Error Rate	*E – n (* = 1 to 9, n = 3 to 12), Upper limit is 3.0E–3
Symbol/Burst	Symbol, Burst Burst Length: 1 to 256/1 Step
Error Addition Method	Type6: Level 0 → Level 2, Level 1 → Level 0, Level 2 → Level 0

Data Output*1

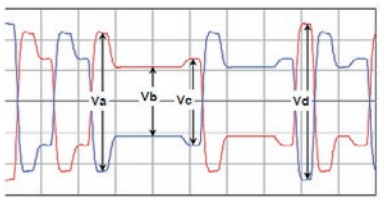
Upper limit baud rate options*1, *2, *3 are required.

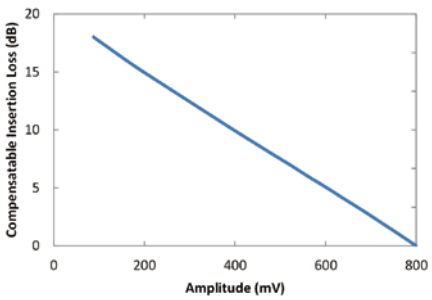
Number of Outputs	1
Waveform	The following measurement conditions are assumed unless otherwise noted. A 100 GHz bandwidth sampling oscilloscope is used. 0.5 Vp-p (NRZ/PAM4) The applicable part J1790A is used.
Coding	NRZ, PAM4, PAM3
Total Amplitude	Note: The lower limit amplitude that creates an error free condition when the output signal is input directly to the ED depends on the performance of the ED in use.
Setting Range	NRZ: 70 mVp-p to 800 mVp-p, 2 mV step (Single-ended) PAM4: 70 mVp-p to 800 mVp-p, 1 mV step (Single-ended) PAM3: 48 mVp-p to 532 mVp-p, 1 mV step (Single-ended)
Accuracy	NRZ and PAM4*4, *5 ± (35 mV + 12% of Total Amplitude) PAM3*6, *7 ± (35 mV + 12% of Total Amplitude)
PAM4 (0/1, 1/2, 2/3Level) Independent variable function	Provided, 20 to 50%, 1 mV Step (Eye amplitude conversion) (PAM4 Amplitude 0/3 level is assumed to be 100%)
Setting Range	PAM4 (0/1Level), (1/2Level), (2/3Level): 23 mV to 266 mVp-p, 1 mV step (Single-ended)
Accuracy	± (35 mV + 12% of Eye Amplitude*8, *9
Offset	
Offset criterion	Vth
Setting Range	–2.0–Eye Amplitude/2 to +3.3–Eye Amplitude/2 Vth, 1 mV step (Single-end)
Accuracy	±65 mV ±10% of offset (Vth) + (Total Amplitude Accuracy/2))
Cross Point	50% Fixed (Typ.)
Tr/Tf	When using the J1789A: 6.0 ps (20 to 80%) (Typ) at 32, 64Gbaud When using the J1790A: 7.0 ps (20 to 80%) (Typ) at 32, 64Gbaud A 100 GHz bandwidth sampling oscilloscope is used.
Half Period Jitter	
Setting Range	–20.0 to +20.0, 0.1 step
Accuracy	±0.04 UI (Typ.)
Jitter	Defined under the following conditions NRZ, 32, 64*1 Gbit/s MU191000A + MU181500B or MG369xA/B/C + MU181500B Clock Input 8 GHz
Intrinsic RJ	≤108 fs rms Calculated by the RJ (rms) of the jitter analysis function using a 01 repetition pattern; specified at 64 Gbit/s. A 100 GHz bandwidth sampling oscilloscope is used.
Jitter RMS	≤600 fs rms Measured in Eye Mode when the Jitter RMS count is 30; specified by PRBS31. A 70 GHz bandwidth sampling oscilloscope is used.

Peak-to-Peak Jitter	≤6 ps p-p Measured at 30 counts of Jitter P-P, as defined by PRBS31. A 70 GHz bandwidth sampling oscilloscope is used.
Random Noise	≤4.75 mVrms Using a 01 repetition pattern, calculated by the RN (rms) of the jitter analysis function, and specified at 64 Gbit/s.
Waveform Distortion (0-peak)	Within ±110 mV (NRZ 32, 64*1 Gbit/s)
PAM4 Level Separation Mismatch Ratio (RLM)	≥0.95 ≥0.975 (Adjustable.) 800 mVp-p/Differential, 32, 64 Gbaud
PAM4 Signal to noise and distortion ratio (SNDR)	PCIe7*10 (PAM4): typ. 35 dB USB4 Gen4*11 (PAM3): typ. 41 dB
Electrical TDECQ	typ.0.9 dB 64 Gbaud
Output ON/OFF	ON/OFF switching
Glitch-free	ON/OFF switching Initiates glitch-free operation without interrupting the PPG output when the frequency fluctuates.
Data/$\overline{\text{Data}}$ Skew	±1 ps Cable error not included.
Termination	AC, DC switching For DC: GND, –2 V, +1.3V, +3.3V, Open (LVDS), 50Ω
Connector	V (J)
Level Guard	Amplitude, Voh and Vol can be set.
External ATT Factor	–40 to 0 dB, 0.1 dB step When the fixed attenuator is connected, the amplitude and offset of the signal output via the fixed attenuator are displayed.

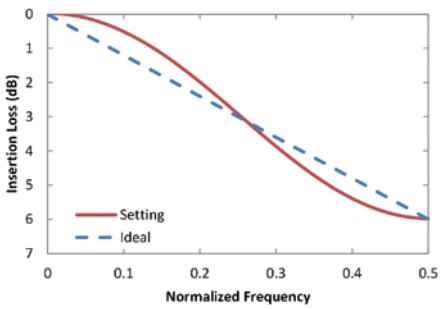
*1: When the Option 001 is installed.
*2: When the Option 002, 112 is installed.
*3: When the Option 003, 113, 123 is installed.
*4: When using the J1789A, Setting Range ≤700 mVp-p
*5: When using the J1790A, Setting Range ≤700 mVp-p (≤32.1 Gbaud)Setting Range ≤650 mVp-p (32.1 < Baud rate ≤ 64.2 Gbaud)
*6: When using the J1789A, Setting Range ≤466 mVp-p
*7: When using the J1790A, Setting Range ≤466 mVp-p (≤32.1 Gbaud)Setting Range ≤433 mVp-p (32.1 < Baud rate ≤ 64.2 Gbaud)
*8: When using the J1789A, Setting Range ≤234 mVp-p
*9: When using the J1790A, Setting Range ≤234 mVp-p (≤32.1 Gbaud)
Setting Range ≤218 mVp-p (≤32.1 < Baud rate ≤ 64.2 Gbaud)
*10: When performing calibration under the following conditions and removing the residual noise of the oscilloscope:
Amplitude: 0.8 Vp-p/Differential, using Pick OFF Tee J1793A, Test Pattern: PRBS13Q
*11: When performing calibration under the following conditions and removing the residual noise of the oscilloscope:
Amplitude: 1.0 Vp-p/Differential, observed with a real-time oscilloscope.

Emphasis (Option 011)

Emphasis Tap	4 tap
Cursor Setting Range/Step	Coeficient: –2.0000 to +2.0000, 0.0001 step De-Emphasis: –20 to +20 dB, 0.01 dB step Post-Cursor: $20*\log_{10}$ (Va/Vb), Pre-Cursor: $20*\log_{10}$ (Vc /Vb)  The coefficient of each tap is the same for Upper Eye, Middle Eye, and Lower Eye. This means that the tap coefficients for Upper Eye, Middle Eye, and Lower Eye cannot be manipulated independently.
Accuracy	± (35 mV + 10% of Total Amplitude x Coeficient)
Setting Range of Emphasis Peak Voltage	max. 800 mVp-p (Single-ended) (NRZ, PAM4) max. 532 mVp-p (Single-ended) (PAM3)
Emphasis ON/OFF	ON/OFF switching

Channel Emulator	Normal: Emulates and outputs a waveform in which a transmission path equivalent to the loaded S-parameters is connected to the PPG output data signal. Inverse: Emulates and outputs a waveform in which the inverse characteristics of a transmission path equivalent to the loaded S-parameters are connected to the PPG output data signal. Intended for use in compensating for transmission path loss. The following graph shows typical limit values for compensable insertion loss. It does not guarantee that all responses emulated from S-parameter files will be compensated in the same manner as the characteristics shown in this graph. 
Response	Normal, Inverse
S-Parameter File	S2 P File (*.s2p file extension), S4 P File (*.s4p file extension) Corresponds to the S2P and S4P output files of the Vector Network Analyzer MS4640B Series.
Channel Emulator ON/OFF	ON/OFF switching
Gain Adjust	When Response is Normal, the amount of loss emulated at the specified frequency is combined with the amount of loss of the read S-Parameter file. 0 GHz/1 GHz/Nyquist Frequency selection

Adjustable ISI (Option 040)

Adjustable ISI	Sets ISI generation channel loss and outputs emulated waveform at PPG Data output signal (output waveform amplitude normalized as set amplitude)
Loss Channel	This can be used by combining the MU196020C with one of the following: Not Specified: External loss channel board J1800A x1 Short Channel: Applicable part J1800A J1800A x2 Middle Channel: Two applicable parts J1800A J1800A x3 Long Channel: Three applicable parts J1800A J1758A: Applicable part J1758A MU195050A Noise: MU195050A Noise Module J1793A Pick OFF Tee: Applicable part J1793A Pick OFF Tee
Frequency	Insertion loss can be set for Nyquist and 1/2 Nyquist Frequency.
Insertion Loss Setting	Displays the absolute loss obtained by adding the amount of loss selected in Loss Channel and the set Tuning Insertion Loss value for Nyquist Frequency and 1/2 Nyquist Frequency.
Tuning Insertion Loss	The absolute loss obtained from the loss value of Loss Channel can be set. –8.00 to 8.00 dB, 0.01 dB step @Nyquist Frequency –8.00 to 8.00 dB, 0.01 dB step @1/2 Nyquist Frequency
Insertion Loss Accuracy	±1.0 dB Nominal @Nyquist Frequency 6 dB, 1,0 repetition pattern, Baud Rate 26.6 GBaud*1, Eye Amplitude 0.5 Vp-p, at each spectrum ±1.5 dB Nominal @Nyquist Frequency 6 dB, 1,0 repetition pattern, Baud Rate 53.1 GBaud*2, Eye Amplitude 0.5 Vp-p, at each spectrum ±1.0 dB Nominal @1/2Nyquist Frequency 3 dB, 1,1,0,0 repetition pattern, Baud Rate 26.6 GBaud*1, Eye Amplitude 0.5 Vp-p, at each spectrum ±1.5 dB Nominal @1/2Nyquist Frequency 3 dB, 1,1,0,0 repetition pattern, Baud Rate 53.1 GBaud*2, Eye Amplitude 0.5 Vp-p, at each spectrum Each specified at constant temperature of 20°C to 30°C The ideal frequency response of insertion loss when Nyquist Frequency is set to 6 dB and 1/2 Nyquist Frequency is set to 3 dB is as shown in the graph below. 
Adjustable ISI ON/OFF	ON/OFF switching

*1: When Options 001, 002, 012, 003, 013, and 023 are installed
*2: When Options 002, 012, 003, 013, and 023 are installed

Insertion Loss Compensation

Insertion Loss Compensation	When Options 011 and 045 are installed When Modulation is set to PAM3 and Baud Rate is set to USB4 Gen4 The Insertion Loss of Nyquist Frequency is compensated for by Emphasis.
Setting Range	0.0 to 2.0 dB/0.1 dB Step
Insertion Loss Accuracy	Since BERT Insertion Loss* is calibrated using an oscilloscope, the accuracy of this value is not guaranteed; the set value is Typ.
Insertion Loss Compensation	ON/OFF switching

*1: BERT Insertion Loss is the standard required for a measuring instrument in the USB4 Version 2 GEN4 Electrical Compliance Test Specification (CTS).

Clock Output

These values are monitored using an applicable part (Coaxial Cable J1439A, 0.8 m, K connector) at a sampling oscilloscope bandwidth of 70 GHz.

Frequency	The operation range is determined according to the upper limit baud rate option.
Full Rate	Operation Baud Rate = Clock Output Frequency 2.4 GHz to 32.1 GHz (Option 001)
Half Rate	Operation Baud Rate = (Clock Output Frequency) × 2 1.2 GHz to 16.05 GHz (Option 001) 1.2 GHz to 29.1 GHz (When the Options 002 and 112 are installed) 1.2 GHz to 32.1 GHz (When the Options 003, 113 and 123 are installed)
Quarter Rate	Operation Baud Rate = (Clock Output Frequency) × 4 0.6 GHz to 8.025 GHz (Option 001) 0.6 GHz to 14.55 GHz (When the Options 002 and 112 are installed) 0.6 GHz to 16.05 GHz (When the Options 003, 113 and 123 are installed)
Number of Output	1
Amplitude	Min. 0.3 Vp-p Max. 1.0 Vp-p (Output Frequency ≤ 16.05 GHz) Min. 0.4 Vp-p Max. 1.0 Vp-p (Output Frequency > 16.05 GHz)
Output Control	ON/OFF switching
Termination	50Ω, AC Coupling
Connector	K (J)

Data Delay

When Option 030 is available.

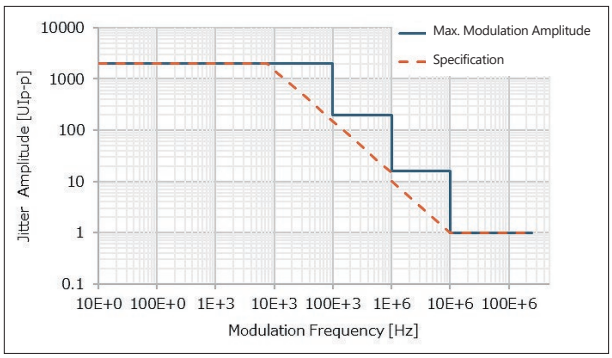
Phase Variable Range	–1000 mUI to +1000 mUI, 2 mUI step
Accuracy	Typ. ±50 mUIp-p* (Baud rate ≤ 32.1 Gbaud) Typ. ±100 mUIp-p* (Baud rate > 32.1 Gbaud)
mUI-ps Switching	Available (internally converted into ps)
Calibration	Available (when jitter modulation is off)
Calibration Indicator	Displayed on the screen when 1/1 clock frequency has changed by ±250 kHz or the temperature around the instrument has changed by ±5°C since the last calibration.

*: The following measurement conditions apply.
A 70 GHz bandwidth sampling oscilloscope is used; Eye Amplitude 0.5 Vp-p (NRZ/PAM4); applicable part J1790A is used.

Jitter tolerance

PCIe 5/6

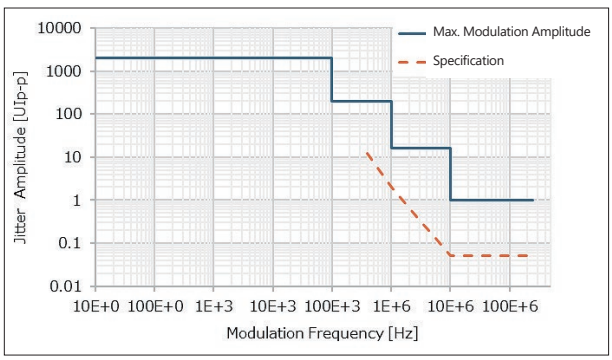
Baud rate 32.0 Gbaud
PRBS2[31] – 1, PAM4
When SSC 33 kHz 5300 ppm Down Spread and RJ 500 fs rms are applied simultaneously by MU181500B



Modulation Frequency [Hz]	Max. Modulation Amplitude [UIp-p]	Specification [UIp-p]
10	2000.0	2000.0
7 500	2000.0	2000.0
10 000	2000.0	1500.0
100 000	2000.0	150.0
1 000 000	200.0	15.0
10 000 000	16.0	1.0
150 000 000	1.0	1.0

PCIe 7

Baud rate 64.0 Gbaud
PRBS2[31] – 1, PAM4
SSC 33 kHz 5300 ppm Down Spread and RJ 125 fs rms are applied simultaneously by MU181500B; defined at the point where Modulation Frequency ≥400 kHz and BER < 1E-12.



Modulation Frequency [Hz]	Max. Modulation Amplitude [UIp-p]	Specification [UIp-p]
10	2000.0	
7 500	2000.0	
100 000	2000.0	
400 000	200.0	12.47
1 000 000	200.0	2.00
10 000 000	16.0	0.05
100 000 000	1.0	0.05
150 000 000	1.0	0.05

$$\frac{1.9156 \times 10^{12}}{F^{1.9969}} \quad (400\ \text{kHz} \le F < 1\ \text{MHz})$$

$$\frac{8.192 \times 10^{9}}{F^{1.6021}} \quad (1\ \text{MHz} \le F < 10\ \text{MHz})$$

$$0.05 \quad (F \le 10\ \text{MHz})$$

(Same as the standard value of F ≥400 kHz or more specified in PCI Express® Base Specification Revision 7.0)

Reference: PCI Express® Base Specification Revision 7.0
The PCIe7 jitter tolerance standard is shown below. The above standard reflects the standard value of 400 kHz or more as is. The standard value of 480 UI at the modulated frequency of 33 kHz corresponds to SSC 33 kHz 5000 ppm. The above standard does not reflect the SJ 33 kHz standard. This is because, in the above standard, SJ is applied after SSC 33 kHz 5300 ppm is applied and, therefore, the PCIe standard is met without applying SJ 33 kHz.

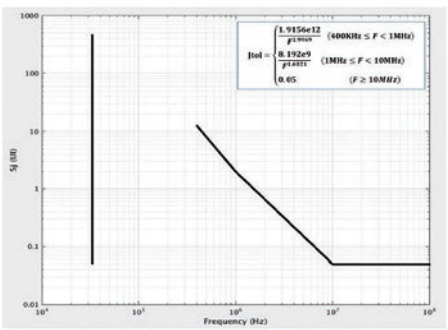
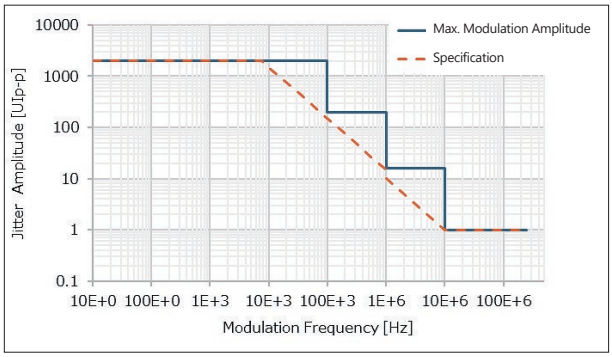


Figure 8-54 Sj Mask for Receivers Operating in SRIS mode at 64.0 and 128.0 GT/s

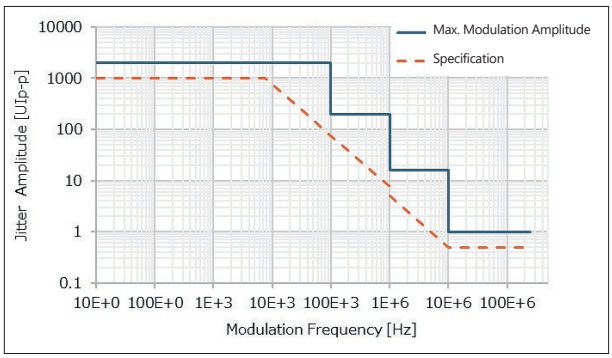
PAM4 PPG MU196020C Specifications

Ethernet 26G	Baud rate 26.5625 Gbaud PRBS2[31] – 1, PAM4 or NRZ



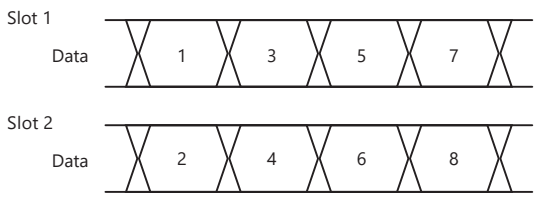
Modulation Frequency [Hz]	Max. Modulation Amplitude [UIp-p]	Specification [UIp-p]
10	2000.0	2000.0
7 500	2000.0	2000.0
10 000	2000.0	1500.0
100 000	2000.0	150.0
1 000 000	200.0	15.0
10 000 000	16.0	1.0
150 000 000	1.0	1.0

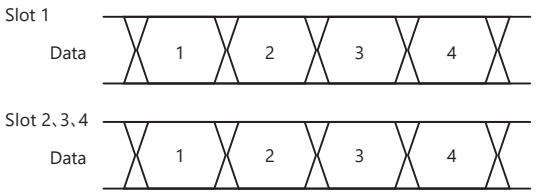
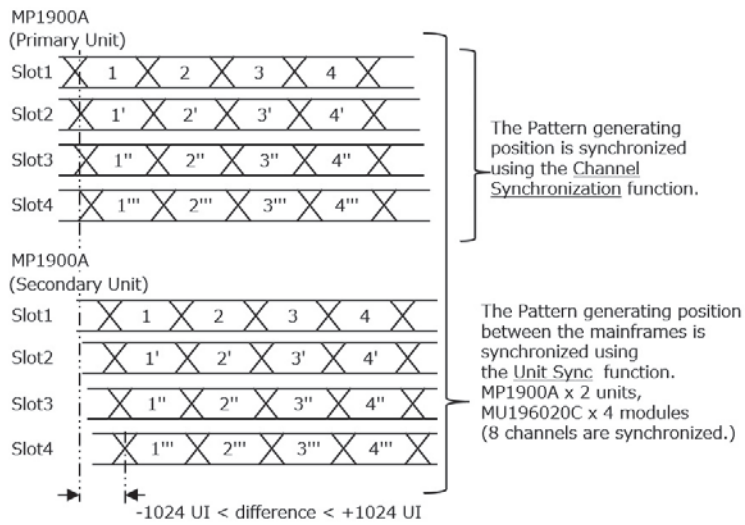
Ethernet 53G	Baud rate 53.125 Gbaud PRBS2[31] – 1, PAM4 or NRZ



Modulation Frequency [Hz]	Max. Modulation Amplitude [UIp-p]	Specification [UIp-p]
10	2000.0	1000.0
7 500	2000.0	1000.0
10 000	2000.0	750.0
100 000	2000.0	75.0
1 000 000	200.0	7.5
10 000 000	16.0	0.5
150 000 000	1.0	0.5

Multichannel Operation (Option 030 or 050)

Inter-Module Synchronization Setting	When Options 030 and 050 are installed Baud Rate ≤ 32.1 Gbaud: Bits can be generated simultaneously with an accuracy of less than 1 UI. Baud Rate > 32.1 Gbaud: Bits can be generated simultaneously with an accuracy of less than 5 UI. Combination setting conditions • Option 001, Option 002 or 012, and Option 003, 013, or 023 must be the same in the modules to be synchronized. • Slots 1 to 2: Inter-Module 2ch Combination (NRZ only) • Slots 1 to 4: Inter-Module CH Synchronization • The modules to be synchronized must be installed consecutively from Slot 1. • The bit generation timing is guaranteed when the temperature is within +/-3□ of the temperature at the time of multi calibration.
Inter-Module 2ch Combination	This can be set for NRZ only. Signals are generated with the first bit generated simultaneously for the modules; and Bits are interleaved between the module. Target application: CEI-112G-NRZ (56 Gbit/s × 2ch), etc. (not mentioned in the catalog)  Inter-Module 2ch Combination

Inter-Module CH Synchronization	Signals are generated with the first bit generated simultaneously for the modules. Target application: 400 GbE (53.125 Gbaud x 4-ch), CEI-112G-PAM4 (56 Gbaud × 4ch), etc. (not mentioned in the catalog)  Inter-Module CH Synchronization
Setting	Only changes to CH Combination and CH Synchronization are mentioned. Unmentioned parts are the same as the Sync OFF operation.
Output	Common to CH Combination and CH Synchronization
Delay	Phase setting range: –64,000 mUI to +64,000 mUI (for each channel independently) Phase setting resolution: 2 mUI (for each channel independently)
Pattern	
Data	Data Length CH Combination: 4 to 536, 870, 912 bits; 2-bit step CH Synchronization: Same as Sync OFF
Unit Sync	ON/OFF switching Valid for MX190000A 3.02.00 or later This can be set when Options 30 and 50 are installed. Valid only when Inter Module Synchronization is executed.
Number of Unit	Synchronization control is possible between up to two chassis (PAM4 PPG (MU196020C) × 4 units × 2 chassis = up to 8 channels can be controlled simultaneously)
Unit Sync Output	Pressing the Unit Sync button outputs the timing signal from the Gating Out connector. The synchronization status between chassis is monitored and indicated. When it is necessary to align the timing, the LED of the Unit Sync button (orange) lights. Valid only when Unit Sync is ON.
Unit Sync Input	Inputs the timing signal from the AUX In connector. Valid only when Unit Sync is ON.
Bit Phase Difference Between Units	Within ±1024 UI Difference in the bit generation timing when the Unit Sync button is pressed 

General

Dimensions and Mass	234 (W) × 21 (H) × 175 (D) mm (Protrusions excluded), 2.5 kg max.
Operating Temperature	+15°C to +35°C MP1900A's ambient temperature. MU196040A shall operate when installed.
Storage Temperature	–20°C to +60°C MU196040A installed to MP1900A shall comply with MIL-T-28800E Class 5.

Operating Baud Rate

<table>
<tr><td>Operating Baud Rate</td><td>When the Option 001 is installed.
2.4 to 32.1 Gbaud
When the Option 002 or 112 is installed.
2.4 to 58.2 Gbaud
When the Option 003, 113, or 123 is installed.
2.4 to 64.2 Gbaud</td></tr>
<tr><td>Operating Baud Rate Setting Range (MU181000B synchronized operation)</td><td>2.400 000 to 25.000 000 Gbaud, 0.000 002 Gbaud step*1, *2, *3
25.000 004 to 32.100 000 Gbaud, 0.000 004 Gbaud step*1, *2, *3
25.000 004 to 50.000 000 Gbaud, 0.000 004 Gbaud step*2, *3
50.000 008 to 58.200 000 Gbaud, 0.000 008 Gbaud step*2
50.000 008 to 64.200 000 Gbaud, 0.000 008 Gbaud step*3
Offset Setting Range/Step
–1000 to +1000 ppm, 1 ppm step*4</td></tr>
<tr><td>Operating Baud Rate Setting Range (MU181000B and MU181500B synchronized operation)</td><td>2.400 000 to 3.125 000 Gbaud, 0.000 002 Gbaud step*1, *2, *3
3.200 002 to 6.250 000 Gbaud, 0.000 002 Gbaud step*1, *2, *3
6.400 002 to 12.500 000 Gbaud, 0.000 002 Gbaud step*1, *2, *3
12.800 002 to 25.000 000 Gbaud, 0.000 002 Gbaud step*1, *2, *3
25.600 004 to 32.100 000 Gbaud, 0.000 004 Gbaud step*1, *2, *3
25.600 004 to 50.000 000 Gbaud, 0.000 004 Gbaud step*2, *3
51.200 008 to 58.200 000 Gbaud, 0.000 008 Gbaud step*2
51.200 008 to 64.200 000 Gbaud, 0.000 008 Gbaud step*3
Offset Setting Range/Step
–1000 to +1000 ppm, 1 ppm step*4</td></tr>
<tr><td>Operating Baud Rate Setting Range (with external clock source)</td><td>Clock Output Rate Full Rate
<table>
<tr><th>Baud Rate Setting Range</th><th>Input Clock Frequency</th><th>Relationship Between Baud Rate and Input Clock Frequency</th></tr>
<tr><td>2.4 to 16.05 Gbaud*1, *2, *3</td><td>2.4 GHz to 16.05 GHz</td><td>Operate at 1/1 clock</td></tr>
<tr><td>16.05 to 32.1 Gbaud*1, *2, *3</td><td>8.025 GHz to 16.05 GHz</td><td>Operate at 1/2 clock</td></tr>
<tr><td>25.0 to 32.1 Gbaud*1, *2, *3</td><td>6.25 GHz to 8.025 GHz</td><td>Operate at 1/4 clock</td></tr>
</table>
Clock Output Rate Half Rate, Quarter Rate
<table>
<tr><th>Baud Rate Setting Range</th><th>Input Clock Frequency</th><th>Relationship Between Baud Rate and Input Clock Frequency</th></tr>
<tr><td>2.4 to 32.1 Gbaud*1, *2, *3</td><td>1.2 GHz to 16.05 GHz</td><td>Operate at 1/2 clock</td></tr>
<tr><td>25.0 to 32.1 Gbaud*1</td><td>6.25 GHz to 8.025 GHz</td><td>Operate at 1/4 clock</td></tr>
<tr><td>25.0 to 50.0 Gbaud*2, *3</td><td>6.25 GHz to 12.50 GHz</td><td>Operate at 1/4 clock</td></tr>
<tr><td>32.1 to 58.2 Gbaud*2</td><td>8.025 GHz to 14.55 GHz</td><td>Operate at 1/4 clock</td></tr>
<tr><td>32.1 to 64.2 Gbaud*3</td><td>8.025 GHz to 16.05 GHz</td><td>Operate at 1/4C clock</td></tr>
<tr><td>50.0 to 58.2 Gbaud*2</td><td>6.25 GHz to 7.275 GHz</td><td>Operate at 1/8 clock</td></tr>
<tr><td>50.0 to 64.2 Gbaud*3</td><td>6.25 GHz to 8.025 GHz</td><td>Operate at 1/8 clock</td></tr>
</table></td></tr>
<tr><td>Operating Baud Rate Setting Range (MU181500B synchronized operation with external clock source)</td><td>Clock Output Rate Full Rate
<table>
<tr><th>Baud Rate Setting Range</th><th>Input Clock Frequency</th><th>Relationship Between Baud Rate and Input Clock Frequency</th></tr>
<tr><td>2.4 to 15.0 Gbaud*1, *2, *3</td><td>2.4 GHz to 15.0 GHz</td><td>Operate at 1/1 clock</td></tr>
<tr><td>15.0 to 30.0 Gbaud*1, *2, *3</td><td>7.5 GHz to 15.0 GHz</td><td>Operate at 1/2 clock</td></tr>
<tr><td>25.0 to 32.1 Gbaud*1, *2, *3</td><td>6.25 GHz to 8.025 GHz</td><td>Operate at 1/4 clock</td></tr>
</table>
Clock Output Rate Half Rate, Quarter Rate
<table>
<tr><th>Baud Rate Setting Range</th><th>Input Clock Frequency</th><th>Relationship Between Baud Rate and Input Clock Frequency</th></tr>
<tr><td>2.4 to 30.0 Gbaud*1, *2, *3</td><td>1.2 GHz to 15.0 GHz</td><td>Operate at 1/2 clock</td></tr>
<tr><td>30.0 to 32.1 Gbaud*1</td><td>7.5 GHz to 8.025 GHz</td><td>Operate at 1/4 clock</td></tr>
<tr><td>30.0 to 58.2 Gbaud*2</td><td>7.5 GHz to 14.55 GHz</td><td>Operate at 1/4 clock</td></tr>
<tr><td>30.0 to 60.0 Gbaud*3</td><td>7.5 GHz to 15.0 GHz</td><td>Operate at 1/4 clock</td></tr>
<tr><td>60.0 to 64.2 Gbaud*3</td><td>7.5 GHz to 8.025 GHz</td><td>Operate at 1/8 clock</td></tr>
</table></td></tr>
</table>

*1: When the Option 001 is installed.
*2: When the Option 002 or 112 is installed.
*3: When the Option 003, 113, or 123 is installed.
*4: Offset setting range depends on the bit rate. The range is -1000 to 0 ppm at the following bit rate.
Full Rate: 12.500 000 Gbaud, 25.000 000 Gbaud
Half Rate, Quarter Rate: 25.000 000 Gbaud, 50.000 000 Gbaud

PAM4 PPG MU196020A Specifications

External Clock Input

Number of Input	1 (Single-end)
Input Frequency Range	1.2 GHz to 16.05 GHz
Input Amplitude	0.3 Vp-p to 1.0 Vp-p (–6.5 to +4.0 dBm)
Termination	50Ω, AC Coupling
Connector	SMA (f)

Aux Input

Number of Input	1 (Single-end)
Variation	Error Injection, Burst
Minimum Pulse Width	1/256 of data rate
Input level	• 0/–1V (H: –0.25 V to 0.05 V, L: –1.1 V to –0.8 V) • 0/–0.5 V (H: –0.05 V to 0.05 V, L: –0.55 V to –0.45 V) • Vth 0 V (Input amplitude: 0.5 Vp-p to 1.0 Vp-p) Select one of the above.
Termination	GND, 50Ω
Connector	SMA (f)

Aux Output

Number of Output	2 (Differential)
Output Control	ON/OFF switching
Variation	1/n Clock (n = 8, 12, 16, 20 … 1020, 1024), Pattern Sync, Burst Out2
Pattern Sync	PRBS, PRGM Position: 1 to {(Least common multiple of Pattern Length' and 256) –263}, in 8 steps When the pattern length is 1023 bits or less, Pattern Length' is the length as an integer multiple so that it becomes 1024 bits or more.
Burst Out2	
Burst Trigger Delay	0 to (Burst Cycle – 256) bits, 8 bits step
Pulse Width	16 bits to (Burst Cycle – 256) bits, 8 bits step
Output Level	0/–0.6 V (H: –0.25 V to 0.05 V, L: –0.80 V to –0.45 V)
Termination	GND, 50Ω
Connector	SMA (f)

Gating Output

Number of Output	1 (Single-end)
Output Control	ON/OFF switching
Variation	Burst, Repeat
Burst	Burst Output
Burst Trigger Delay	0 to (Burst Cycle – 256) bits, 8 bits step
Enable Pulse Width	16 bits to (Burst Cycle – 256) bits, 8 bits step
Output Level	0/–1 V (H: –0.25 V to 0.05 V, L: –1.25 V to –0.8 V) *
Repeat	Timing Signal Output
Timing Signal Cycle	$\mathrm{INT}\left(\frac{\text{Pattern}}{\text{length}}\right) \times 256$
Timing Signal Delay	0 to {(Least common multiple of Pattern Length' and 256) –256} The maximum settable number is 68 719 476 480, in 8- bit steps. When the pattern length is 1023 bits or less, Pattern Length' is the length as an integer multiple so that it becomes 1024 bits or more.
Timing Signal Pulse Width	256 to {(Least common multiple of Pattern Length' and 256) –256} The maximum settable number is 68 719 476 480, in 8- bit steps. When the pattern length is 1023 bits or less, Pattern Length' is the length as an integer multiple so that it becomes 1024 bits or more.
Output Level	0/–1 V (H: –0.25 V to 0.05 V, L: –1.25 V to –0.8 V) *
Termination	GND, 50Ω
Connector	SMA (f)

*: L: Output Enable, H: Output Disable

PAM4 PPG MU196020A Specifications

Generated Pattern*1

PRBS	
Pattern Length	$2^n - 1$ (n = 7, 9, 10, 11, 13, 15, 20, 23, 31)
Mark Ratio	1/2 (1/2INV is supported by a logical inversion.)
PRBS Generator Polynomial	n = 7: $1 + X^6 + X^7$ n = 9: $1 + X^5 + X^9$ n = 10: $1 + X^7 + X^{10}$ n = 11: $1 + X^9 + X^{11}$ n = 13: $1 + X + X^2 + X^{12} + X^{13}$ n = 15: $1 + X^{14} + X^{15}$ n = 20: $1 + X^3 + X^{20}$ n = 23: $1 + X^{18} + X^{23}$ n = 31: $1 + X^{28} + X^{31}$
PRBS Inversion	This is available in PAM4 mode only. Logical inversion of PRBS can be set independently for MSB and LSB.
Zero-Substitution	This is available in NRZ mode only.
Additional Bit	0 bit, 1 bit
Pattern Length	2^n or $2^n - 1$ (n = 7, 9, 10, 11, 15, 20, 23)
Start Position	Substitutes the bit coming after the maximum "0" successive bits.
Length of Consecutive Zero Bits	1 bits to (Pattern Length – 1) bits If the bit coming after Zero-substitution is "0", then it is replaced with "1".
Data	
Data Length	NRZ: 2 bits to 268 435 456 bits, 1 bit step PAM4: 2 to 268 435 456 symbols, 1 symbol step
Bit Shift	This is available in PAM4 mode only. Bit shift of MSBs can be controlled in the range of ±256 bits (in 1-bit steps).
PAM4 Standard Pattern	Standard-compliant PAM4-mode patterns
CEI	QPRBS13-CEI, QPRBS31-CEI
IEEE	IEEE802.3bs/cd: PRBS13Q, PRBS31Q, SSPRQ, Square Wave IEEE802.3bj: QPRBS13, JP03A, JP03B, Transmitter Linearity
RS-FEC (Option 042)	RS-FEC Scrambled Idle 50G 1 Lane (26.5625 Gbaud, 50GBASE-KR/CR/SR/FR/LR) RS-FEC Scrambled Idle 100G 1 Lane (53.125 Gbaud, 100GBASE-DR/KR1/CR1) RS-FEC-Int Scrambled Idle 100G 1 Lane (53.125 Gbaud, 100GBASE-P) RS-FEC Scrambled Idle 100G 2 Lanes (26.5625 Gbaud, 100GBASE-KR2/CR2/SR2) RS-FEC Scrambled Idle 200G 4 Lanes (26.5625 Gbaud, 200GBASE-SR4/DR4/FR4/LR4) RS-FEC Scrambled Idle 200G 2 Lanes (53.125 Gbaud, 200GBASE-KR2/CR2) RS-FEC Scrambled Idle 400G 4 Lanes (53.125 Gbaud, 400GBASE-DR4/KR4/CR4) RS-FEC Scrambled Idle 400G 8 Lanes (26.5625 Gbaud, 400GBASE-FR8/LR8)
InfiniBand	PRBS13Q (InfiniBand), PRBS23Q, PRBS31Q (InfiniBand)
Fibre Channel	PRBS31Q (Fibre Channel)
NRZ Standard Pattern	Standard-compliant NRZ-mode pattern
CEI	SSPR
RS-FEC (Option 042)	RS-FEC Scrambled Idle 25G 1 Lane (25.78125 Gbaud, 25GBASE-KR/CR/SR/LR/ER) RS-FEC Scrambled Idle 50G 2 Lanes RS (544, 514) (26.5625 Gbaud, 50GAUI-2) RS-FEC Scrambled Idle 100G 4 Lanes (25.78125 Gbaud, 100GBASE-KR4/CR4/SR4) RS-FEC Scrambled Idle 100G 4 Lanes RS (544, 514) (26.5625 Gbaud, 100GBASE-KP4)
Sequence*2	
Specification	PCIe1, PCIe2, PCIe3, PCIe4, PCIe5/CXL1-2*3, PCIe6/CXL3*3
Transmit	Starts transmitting the sequence pattern.
Manual	Enabled when Manual Trigger is set.
Trigger Block No.	Sets the block number of the sequence to output an LTSSM Trigger signal from AUX Output connector. 1 to 256 Block No. 1 step

*1: Since the output circuit is DC-terminated using the AC-coupled Bias Tee method, the same symbol pattern has a 50% change in output level over acontinuous period of about 5 µs.
*2: Requires MU196020A-051/351
*3: Requires both MU196020A-051/351 and MU196020A-056/356 options for CXL1-2/3

Pattern Sequence

Sequence	Repeat, Burst
Repeat	Continuous Pattern
Burst	This is available only when Coding is NRZ.
Source	Internal, External-Trigger (Aux Input), External-Enable (Aux Input)
Data Sequence	Restart, Consecutive, Continuous
Enable Period	Internal: 12800 bits to 2 147 483 136 bits, 256 bits step Ext Trigger/Enable: 12800 bits to 2 147 483 648 bits, 256 bits step
Burst Cycle	25600 bits to 2 147 483 648 bits, 1024 bits step

PAM4 PPG MU196020A Specifications

Coding

Coding	NRZ, PAM4
NRZ	Normal, Invert
PAM4 Gray Coding	ON, OFF
PAM4 Precoding (1/ (1 + D) mod 4)*	ON, OFF

*: Generator polynomial compliant with the IEEE802.3

Error Addition

Type	Bit, Error on MSB, Error on LSB, Error on LSB&MSB, RS-FEC Symbol Error (Option 042)
Bit	This is available only when Coding is NRZ.
Burst Error	1 bits to 256 bits
Source	Internal, External-Trigger (Rise edge trigger), External-Disable (L: Disable)
Error Variation	Repeat, Single, (Cannot be selected when Source is External-Trigger.)
Error Rate	*E – n (*= 1 to 9, n = 3 to 12), Upper limit is 3.0E–3
Error Route	Select 1 to 32, Scan
Error on MSB	Adds the specified symbol error. This is available only when Coding is PAM4. The set error is added to MSB only.
Burst Error	1 symbols to 256 symbols
Source	Internal, External-Trigger (Rise edge trigger), External-Disable (L: Disable)
Error Variation	Repeat, Single (Cannot be selected when Source is External-Trigger.)
Symbol Error Rate	*E – n (*= 1 to 9, n = 3 to 12), Upper limit is 3.0E–3
Error on LSB	Adds the specified symbol error. This is available only when Coding is PAM4. The set error is added to LSB only.
Burst Error	1 symbols to 256 symbols
Source	Internal, External-Trigger (Rise edge trigger), External-Disable (L: Disable)
Error Variation	Repeat, Single (Cannot be selected when Source is External-Trigger.)
Symbol Error Rate	*E – n (*= 1 to 9, n = 3 to 12), Upper limit is 3.0E–3
Error on LSB & MSB	Adds the specified symbol error. This is available only when Coding is PAM4. An error is inserted to make the PAM4 signal change by one level only.
Burst Error	1 symbols to 256 symbols
Source	Internal, External-Trigger (Rise edge trigger), External-Disable (L: Disable)
Error Variation	Repeat, Single (Cannot be selected when Source is External-Trigger.)
Symbol Error Rate	*E – n (*= 1 to 9, n = 3 to 12), Upper limit is 3.0E–3
Error Addition Method	Type1: Level 0 → Level 1, Level 1 → Level 2, Level 2 → Level 3, Level 3 → Level 2 Type2: Level 0 → Level 1, Level 1 → Level 2, Level 2 → Level 1, Level 3 → Level 2 Type3: Level 0 → Level 1, Level 1 → Level 0, Level 2 → Level 1, Level 3 → Level 2
RS-FEC Symbol Error (Option 042)	Inserts error to change only one PAM4 signal level NRZ: Inserts error at 10-bit gap PAM4: Inserts error at 10 PAM4 Symbol or 20 PAM4 Symbol gap
Control Method	Internal, External-Trigger (Rising edge trigger), External-Disable (L: Disable)
Addition Method	Repeat, Single, (Can select Variation at Source External-Trigger)
Symbol Error per Code Word	1 to 20
Symbol Error Rate	*E – n (*= 1 to 9, n = 3 to 12), Upper limit is 3.0E–3 Error addition range changes with number of Symbol Errors per Code Word
Error Addition Method (PAM4)	Type1: Level 0 → Level 1, Level 1 → Level 2, Level 2 → Level 3, Level 3 → Level 2 Type2: Level 0 → Level 1, Level 1 → Level 2, Level 2 → Level 1, Level 3 → Level 2 Type3: Level 0 → Level 1, Level 1 → Level 0, Level 2 → Level 1, Level 3 → Level 2

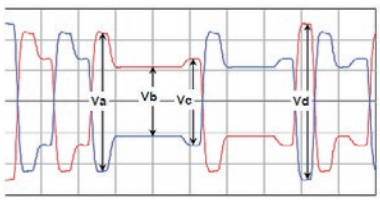
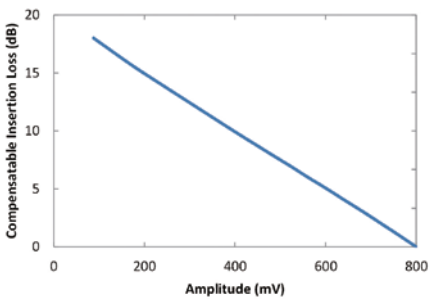
Data Output*1

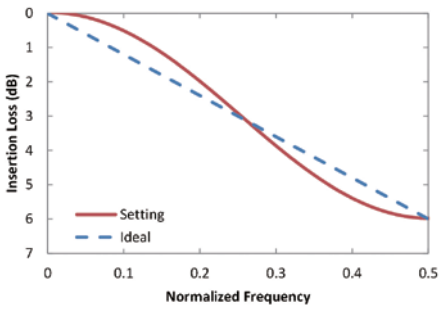
Number of Outputs	2 (Data, XData) Non independent variable
Waveform	NRZ, PAM4
NRZ Eye Amplitude	
Setting Range	NRZ: 70 mVp-p to 800 mVp-p, 2 mV step (Single-end)
Accuracy	When using the J1789A: ±35 mV ±12% (Single-end) *2 When using the J1790A: ±35 mV ±12% (Single-end) *3, *4, *5
PAM4 Eye Amplitude	
PAM4 (0/3 Level) Setting Range	PAM4 (0/3 Level): 70 mVp-p to 800 mVp-p, 1 mV step (Single-end) *6
PAM4 (0/3 Level) Accuracy	When using the J1789A: ±35 mV ±12% of Amplitude*2, *7 When using the J1790A: ±35 mV ±12% of Amplitude*3, *4, *5, *7
PAM4 (0/1, 1/2, 2/3 Level) Independent variable function	Provided, 20 to 50%, 1 mV Step (Eye amplitude conversion) (PAM4 Amplitude 0/3 level is assumed to be 100%)
PAM4 (0/1, 1/2, 2/3 Level) Setting Range	PAM4 (0/1 Level): 23 mVp-p to 266 mVp-p, 1 mV step (Single-end) PAM4 (1/2 Level): 24 mVp-p to 268 mVp-p, 1 mV step (Single-end) PAM4 (2/3 Level): 23 mVp-p to 266 mVp-p, 1 mV step (Single-end)
PAM4 (0/1, 1/2, 2/3 Level) Accuracy	When using the J1789A: ±35 mV ±12% of Amplitude*8 When using the J1790A: ±35 mV ±12% of Amplitude*9, *10, *11
Offset	
Setting Range	–2.0–Eye Amplitude/2 to +3.3–Eye Amplitude/2 Vth, 1 mV step (Single-end)
Accuracy	±65 mV ±10% of offset (Vth) ± (Eye Amplitude Accuracy/2) (Except when Emphasis is turned On with the MU196020A-x11 installed.) (For PAM4, when setting each of PAM4 Amplitude (3/2, 2/1 and 1/0) equally to 33%.)
Cross Point	Typ. 50% (fixed)
Tr/Tf	When using the J1789A: Typ. 8.5 ps (20 to 80%)*12 Typ. 9 ps (20 to 80%)*13 When using the J1790A: Typ. 8.8 ps (20 to 80%)*12 Typ. 9.5 ps (20 to 80%)*13
Half Period Jitter	
Setting Range	–20 to 20, 1step
Accuracy	Typ. ±0.04 UI*14
Jitter	
Measurement conditions	NRZ, Bit rate: 32.1 Gbit/s (When the Option 001 is installed) 58.2 Gbit/s (When the Options 002 and 112 are installed) 64.2 Gbit/s (When the Options 003, 113 and 123 are installed) Eye Amplitude 0.5 Vp-p (Single-end) At a constant temperature between 20°C and 30°C, measure with a 70-GHz bandwidth sampling oscilloscope with residual jitter of less than 200 fs rms.
Peak-to-Peak Jitter	Typ. 6 ps p-p (Count of measured jitters: 30)
Jitter RMS	Typ. 600 fs rms (Count of measured jitters: 30)
Intrinsic RJ (RMS)	Typ. 170 fs (Repeating pattern of 1,0) *15
Waveform Distortion (0-peak)	Typ. ±110 mV*16
PAM4 Level Separation Mismatch Ratio (R_{LM})	0.95 (min.) *17
PAM4 Signal to noise and distortion ratio (SNDR)	33 dB (min.) *18, *19
Electrical TDECQ	0.9 dB*20
Output ON/OFF	ON/OFF switching available
Data/XData Skew	±1 ps Cable error not included.
Termination	AC, DC switching For DC: GND, –2V, +1.3V, +3.3V, Open (LVDS), 50Ω
Connector	V (f)
Offset Reference	Vth
Level Guard	Amplitude, Voh and Vol can be set.
External ATT Factor	–40 to 0 dB, 0.1 dB step When the fixed attenuator is connected, the amplitude and offset of the signal output via the fixed attenuator are displayed.

*1: Unless otherwise specified, these are specified with the conditions of PRBS2^{31} – 1, Mark ratio 1/2, and Cross Point 50%.
The values shall be observed by using an optional accessory, J1789A or J1790A, and a 70-GHz bandwidth sampling oscilloscope.
*2: Setting Range ≤ 700 mVp-p
*3: Setting Range ≤ 700 mVp-p (≤ 32.1 Gbit/s, when the Options 001, 002, 112, 003, 113 and 123 are installed)
*4: Setting Range ≤ 600 mVp-p (≤ 58.2 Gbit/s, when the Options 002, 112, 003, 113 and 123 are installed)

*5: Setting Range ≤ 550 mVp-p (≤ 64.2 Gbit/s, when the Options 003, 113 and 123 are installed)
*6: When inputting the PAM4 output signal directly to the ED, the lower amplitude limit that makes it free from errors depends on the performance of the ED used.
When using MP1862A as ED, the lower amplitude limits (reference data) that make the data to be free from any errors are as follows:
125 mV (0/3 Level, ≤ 32.1 Gbaud, when the Option 001 is installed)
250 mV (0/3 Level, ≤ 58.2 Gbaud, when the Options 002, 112, 003, 113 and 123 are installed)
Pattern: PRBS15, at a constant temperature between 20°C and 30°C
*7: Single-end, PAM4 0/3 Level, and when setting each of PAM4 Amplitude (3/2, 2/1 and 1/0) equally to 33%
*8: Setting Range ≤ 234 mVp-p, Single-end, at each amplitude level (Upper, Middle, Lower)
*9: Setting Range ≤ 234 mVp-p, Single-end, at each amplitude level (Upper, Middle, Lower)
(≤ 32.1 Gbit/s, when the Options 001, 002, 112, 003, 113 and 123 are installed)
*10: Setting Range ≤ 200 mVp-p, Single-end, at each amplitude level (Upper, Middle, Lower)
(≤ 58.2 Gbit/s, when the Options 002, 112, 003, 113 and 123 are installed)
*11: Setting Range ≤ 184 mVp-p, Single-end, at each amplitude level (Upper, Middle, Lower), when using the J1790A coaxial cable (0.8m)
(≤ 64.2 Gbit/s, when the Options 003, 113 and 123 are installed)
*12: NRZ, 58.2 Gbit/s (when the Options 002 and 112 are installed), 64.2 Gbit/s (when the Options 003, 113 and 123 are installed), Eye Amplitude 0.5 Vp-p (Single-end), only when Coding is NRZ and Emphasis is Off.
*13: NRZ, 32.1 Gbit/s, Eye Amplitude 0.5 Vp-p (Single-end), only when Coding is NRZ and Emphasis is Off.
*14: 2.4, 8, 16, 26.562 5, 32.1 Gbit/s (When the Option 001 is installed), 2.4, 8, 16, 26.562 5, 32.1, 40, 53.125, 58.2 Gbit/s (When the Options 002 and 112 are installed)
2.4, 8, 16, 26.562 5, 32.1, 40, 53.125 ,58.2 ,64.2 Gbit/s (When the Options 003, 113 and 123 are installed), Eye Amplitude 0.5 Vp-p (Single-end)
*15: NRZ, Bit rate 58.2 Gbit/s (When the Options 002 and 112 are installed), 64.2 Gbit/s (When the Options 003, 113 and 123 are installed)
*16: NRZ, Bit rate 32.1 Gbit/s (When the Option 001 is installed), 58.2 Gbit/s (When the Options 002 and 112 are installed), 64.2 Gbit/s (When the Options 003, 113 and 123 are installed)
Eye Amplitude 0.5 Vp-p (Single-end)
*17: PAM4, 26.5625 Gbaud (When the Option 001 is installed), 53.125 Gbaud (When the Options 002, 112, 003, 113 and 123 are installed),
1.0 Vp-p (Differential), refer to the IEEE P802.3bs for equation to calculate.
*18: PAM4, 26.5625 Gbaud (When the Option 001 is installed), 53.125 Gbaud (When the Options 002, 112, 003, 113 and 123 are installed),
1.0 Vp-p (Differential), refer to the IEEE P802.3cd for equation to calculate.
*19: 60-GHz bandwidth sampling oscilloscope
*20: 26.5625 Gbaud (When the Option 001 is installed), 53.125 Gbaud (When the Options 002, 112, 003, 113 and 123 are installed),
Using an equalizer, Single, Pattern: SSPRQ

Emphasis (Option 011)

Emphasis Tap	4 (1post-cursor, 2pre-cursor) 4 Tap parameter values for all eyes (Upper, Middle and Lower) become identical. This means that 4 Tap parameters for Upper, Middle and Lower Eyes cannot be controlled independently.
Cursor Setting Range/Step	–20 to +20 dB, 0.1 dB step (Post-Cursol: $20\log_{10}Va/Vb$, Pre-Cursol: $20\log_{10}Vc/Vb$)  Provided that the maximum amplitude is restricted by the setting range of emphasis peak voltage.
Accuracy	Typ. ±1 dB (16 Gbaud, Amplitude 0.5 Vp-p (Single-end), De-Emphasis, Pre-Cursor1 = 6 dB, Post Cursor1 = 3.5 dB)
Setting Range of Emphasis Peak Voltage	70 mVp-p to 800 mVp-p (Single-end)
Channel Emulator (Option 040)	Normal: Outputs signal simulating transmission path equivalent to loaded S-Parameter file at PPG Data Output Inverse: Outputs signal with set De-Emphasis for correcting loss of transmission path equivalent to loaded S-Parameter file at PPG Data Output The following graph shows the maximum transmission path loss correction using the Channel Emulator function without reducing amplitude. 
S-Parameter File	S2P File (*.s2p file extension), S4P File (*.s4p file extension) Supports files output by Vector Network Analyzer MS4640B series
Response	Normal, Inverse
Gain Adjust	At Normal, matches loaded S-Parameter file loss with emulated loss for 0 GHz or 1 GHz or Nyquist Frequency

Adjustable ISI (Option 040)	Sets ISI generation channel loss and outputs emulated waveform at PPG Data output signal (output waveform amplitude normalized as set amplitude) Used in combination with channel board, such as J1800A/J1758A (optional accessories), or Noise Module MU195050A
Insertion Loss Setting	Sets relative loss from Loss Channel for Nyquist and 1/2 Nyquist Frequency –8.00 to 8.00 dB, 0.01-dB step @ Nyquist Frequency –8.00 to 8.00 dB, 0.01-dB step @ 1/2 Nyquist Frequency
Insertion Loss Accuracy	±1.0 dB Nominal @ Nyquist Frequency 6 dB, 26.6 GBaud 1,0 repetition pattern ±1.5 dB Nominal @ Nyquist Frequency 6 dB, 53.1 GBaud 1,0 repetition pattern ±1.0 dB Nominal @ 1/2Nyquist Frequency 3 dB, 26.6 GBaud 1,1,0,0 repetition pattern ±1.5 dB Nominal @ 1/2Nyquist Frequency 3 dB, 53.1 GBaud 1,1,0,0 repetition pattern Each specified at Eye Amplitude = 0.5 Vp-p, and constant temperature of 20°C to 30°C The Insertion Loss characteristics are as follows (ISI Nominal Data) when set Nyquist Frequency = 6 dB and 1/2 Nyquist Frequency = 3 dB. 
Emulator On/Off	Can synthesize any of Channel Emulator, Adjustable ISI, and Emphasis Tap

Clock Output

These values are monitored using an applicable part (Coaxial Cable J1439A, 0.8 m, K connector) at a sampling oscilloscope bandwidth of 70 GHz.

Frequency	
Full Rate	Operation Baud Rate = Clock Output Frequency 2.4 GHz to 32.1 GHz (Option 001)
Half Rate	Operation Baud Rate = (Clock Output Frequency) × 2 1.2 GHz to 16.05 GHz (Option 001) 1.2 GHz to 29.1 GHz (When the Options 002 and 112 are installed) 1.2 GHz to 32.1 GHz (When the Options 003, 113 and 123 are installed)
Quarter Rate	Operation Baud Rate = (Clock Output Frequency) × 4 0.6 GHz to 8.025 GHz (Option 001) 0.6 GHz to 14.55 GHz (When the Options 002 and 112 are installed) 0.6 GHz to 16.05 GHz (When the Options 003, 113 and 123 are installed)
Number of Output	1
Amplitude	Min. 0.3 Vp-p Max. 1.0 Vp-p (Output Frequency ≤ 16.05 GHz) Min. 0.4 Vp-p Max. 1.0 Vp-p (Output Frequency > 16.05 GHz)
Output Control	ON, OFF switching
Termination	50Ω, AC Coupling
Connector	K (f)

Data Delay

When Option x30 is added.

Phase Variable Range	–1000 mUI to +1000 mUI, 2 mUI step
Accuracy	Typ. ±50 mUIp-p*1, *2 Typ. ±100 mUIp-p*1, *3
mUI-ps Switching	Available (internally converted into ps)
Calibration	Available (when jitter modulation is off)
Calibration Indicator	This is displayed when one of the following conditions occur: • 1/1 Clock frequency change by ±250 kHz. • Ambient temperature change by ±5 degree.

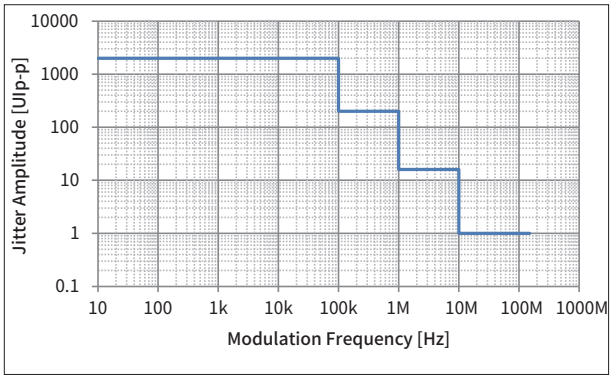
*1: Measured with a sampling oscilloscope with residual jitter of less than 200 fs rms, at a constant amplitude setting.
*2: Baud rate ≤ 32.1 Gbaud
*3: Baud rate > 32.1 Gbaud

Jitter Setting Range

Jitter Setting Range

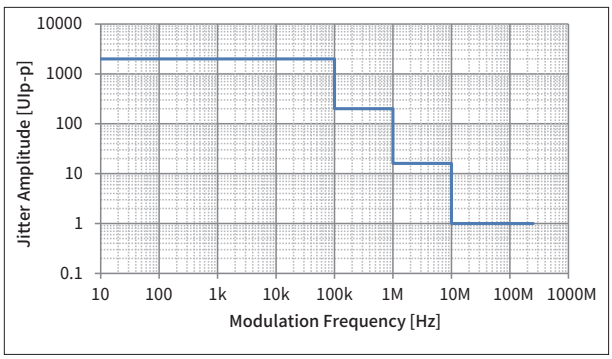
When linking with MU181000A/B and MU181500B
SJ1 Clock Output Rate
At Half Rate, Quarter Rate

60 < Baud rate ≤ 64.2 Gbaud, 30 < Baud rate ≤ 34 Gbaud, 8 < Baud rate ≤ 17 Gbaud



Modulation Frequency [Hz]	Jitter Amplitude [UIp-p]
10 to 100k	0 to 2000
100.1k to 1M	0 to 200
1.001M to 10M	0 to 16
10.01M to 150M	0 to 1

34 < Baud rate ≤ 60 Gbaud, 17 < Baud rate ≤ 30 Gbaud



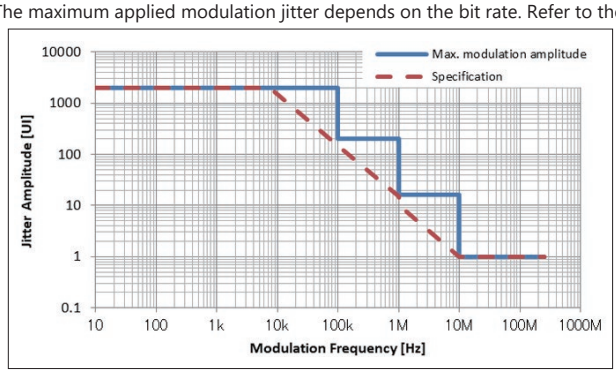
Modulation Frequency [Hz]	Jitter Amplitude [UIp-p]
10 to 100k	0 to 2000
100.1k to 1M	0 to 200
1.001M to 10M	0 to 16
10.01M to 250M	0 to 1

Jitter tolerance

Jitter Tolerance Mask

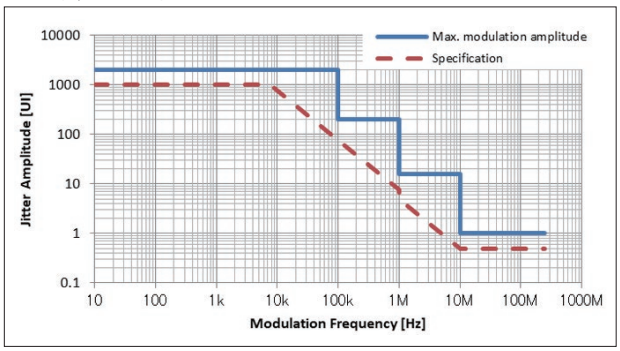
For NRZ output,
Bit rate: 32.1 Gbit/s (Option 001)
58.2 Gbit/s (When the Options 002 and 112 are installed)
64.2 Gbit/s (When the Options 003, 113 and 123 are installed)
Pattern: PRBS2^{31}–1

With MU181500B, SSC with frequency of 33 kHz and deviation of 5300 ppm can be applied simultaneously with RJ with amplitude of 0.3 UI.
These specifications are defined assuming the following conditions:
Loopback connection to MU196040A (32.1 Gbit/s) or MP1862A + MU183040B (58.2 Gbit/s, 64.1 Gbit/s), at a constant temperature between 20°C and 30°C.
When RJ + BUJ is bigger than 0.5 UIp-p or SJ1 + Built-in SJ2 + RJ + BUJ is bigger than the standard value + 0.3 UIp-p, "Overload" is displayed on the MU181500B screen.
The maximum applied modulation jitter depends on the bit rate. Refer to the jitter setting range for details.



Modulation Frequency [Hz]	Max. Modulation Amplitude [UIp-p]	Specification [UIp-p]
10	2,000	2,000
7,500	2,000	2,000
100,000	2,000	150
1,000,000	200	15
10,000,000	16	1
250,000,000	1	1

58.2 Gbit/s, 64.2 Gbit/s



Modulation Frequency [Hz]	Max. Modulation Amplitude [UIp-p]	Specification [UIp-p]
10	2,000	1,000
7,500	2,000	1,000
100,000	2,000	75
1,000,000	200	7.5
10,000,000	16	0.5
250,000,000	1	0.5

Multichannel Operation (Option 030 or 050)

Shared Conditions	Option 001/002/003 can operate between same modules Operation requires both -030 and -050 options. ≤32.1 GBaud: Aligns bit generation timing with <1 UI accuracy* >32.1 GBaud: Aligns bit generation timing with <5 UI accuracy* * The bit generation timing is assured when the change in ambient temperature from that at Multi-Calibration is within ±3°C.
Channel Sync between Modules (Installed in Slot 1 to 4 tracking Slot 1)	Generates signal with bit timing aligned between modules Slot 1 Data 1 2 3 4 Slot 2, 3, 4 Data 1 2 3 4 CH Sync Image
2ch Combination between Modules (Only NRZ, Installed in Slot 1 and 2)	Generates signal with bit timing aligned between modules and bit pattern interleaved between modules Slot1 Data 1 3 5 7 Slot2 Data 2 4 6 8 CH Combination Image Phase Setting: –64,000 mUI to +64,000 mUI, 2-mUI steps (independently for each channel) Pattern Length: 4 to 536,870,912 bits, 2-bit steps

General

Dimensions and Mass	234 (W) × 21 (H) × 175 (D) mm (Protrusions excluded), 2.5 kg max.
Operating Temperature	+15°C to +35°C MP1900A's ambient temperature. MU196040A shall operate when installed.
Storage Temperature	–20°C to +60°C MU196040A installed to MP1900A shall comply with MIL-T-28800E Class 5.

Operating Baud Rate

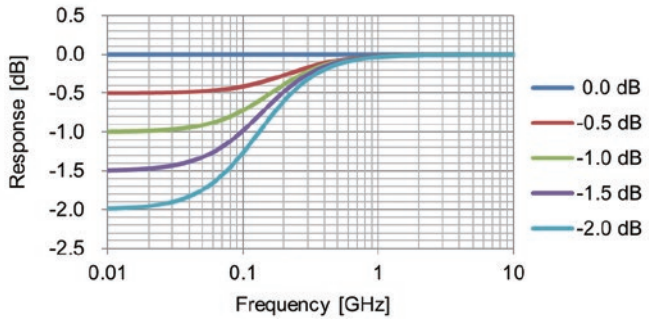
Operating Baud Rate	When the Option 001 is installed. PAM4 input: 2.4 Gbaud to 32.1 Gbaud NRZ input: 2.4 Gbit/s to 32.1 Gbit/s When the Option 002 or 112 is installed. PAM4 input: 2.4 Gbaud to 58.2 Gbaud NRZ input: 2.4 Gbit/s to 64.2 Gbit/s

System Clock

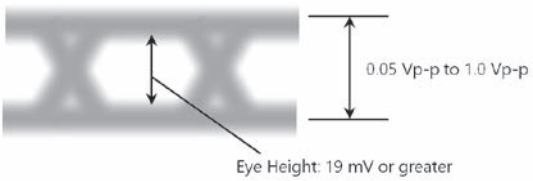
System Clock	External, Recovered Clock (When the Option x21, x22, x23, or x24 is installed) External: Clock input from the Ext Clock Input connector For PAM4, select from 2.4 Gbaud to 32.1 Gbaud, 32.1 Gbaud to 58.2 Gbaud and Auto. For NRZ, select from 2.4 Gbit/s to 32.1 Gbit/s, 32.1 Gbit/s to 64.2 Gbit/s and Auto. Recovered Clock: Clock recovered from the data input from the Data Input connector

Data Input

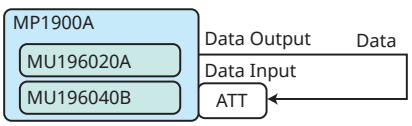
Number of Inputs	2 (Data, $X\overline{Data}$) (Differential)
Input Condition	Single-end, Differential 50Ω, Differential 100Ω When set to Differential 50Ω or Differential 100Ω: Independent, Tracking, Alternate*1 When set to Alternate: Data-XData, XData-Data*2 When set to Single-end: Data, XData*3
Signal Type	NRZ, PAM4
LSB/MSB Diagnostics	When set to PAM4, the PAM4 mode can be switched between as follows: Diagnostics Mode OFF: Treats signals as symbols by receiving LSB and MSB while synchronizing them with each other. Diagnostics Mode ON: Asynchronously receives LSB and MSB.
Input Amplitude	NRZ: The range in which the Auto Adjust function and the Auto Search function operate. 0.05 Vp-p to 1.0 Vp-p*4, *5 0.1 Vp-p to 1.0 Vp-p*4, *6 PAM4: The range in which the Auto Search PAM4 Fine function operates. 0.3 Vp-p to 1.0 Vp-p*7, *8 0.4 Vp-p to 1.0 Vp-p*7, *9
Threshold Voltage	NRZ, PAM4 Middle Eye Threshold: –3.5 V to +3.3 V, 1 mV step*2, *10 PAM4 Upper Eye Threshold: –3.9 V to +3.7 V, 1 mV step*11 PAM4 Lower Eye Threshold: –3.9 V to +3.7 V, 1 mV step*11
Input Sensitivity	Single-Ended, Mark Ratio1/2, PRBS31, when connecting directly to the MU196020A using J1789A and an attenuator, Emphasis ON, unused connectors on the MU196020A and MU196040B are terminated, Error free at a constant temperature between 20°C and 30°C
Eye Amplitude	NRZ Typ. 25 mVp-p, ≤50 mVp-p*12 (26.5625 Gbit/s, 32.1 Gbit/s) Typ. 31 mVp-p, ≤55 mVp-p*13 (53.125 Gbit/s) Typ. 43 mVp-p, ≤60 mVp-p*13 (64.2 Gbit/s)
Eye Height	NRZ Typ. 19 mV*12 (26.5625 Gbit/s, 32.1 Gbit/s) Typ. 21 mV*13 (53.125 Gbit/s) Typ. 32 mV*13 (64.2 Gbit/s) PAM4 0/1 1/2 2/3 Level, PRBS31, when using External Clock Typ. 23 mV, ≤50 mV*12 (26.5625 Gbaud, 32.1 Gbaud) Typ. 36 mV, ≤60 mV*13 (53.125 Gbaud) Typ. 49 mV, ≤70 mV*13 (58.2 Gbaud) Note that 53.125 Gbaud and 58.2 Gbaud are defined by the Eye Height value that results in a differential waveform having BER of 1E-06 by changing the test pattern to QPRBS13-CEI after setting the test pattern to PRBS31 and setting the amplitude value.
Phase Margin	Differential, Mark Ratio 1/2, PRBS31, when inputting 0.5 Vp-p, when connecting directly to the MU196020A using J1789A and an attenuator. Error free at a constant temperature between 20°C and 30°C, when using External Clock NRZ*14 Typ. 25.8 ps*12 (26.5625 Gbit/s) Typ. 18.0 ps*12 (32.1 Gbit/s) Typ. 10.5 ps*13 (53.125 Gbit/s) Typ. 8.7 ps*13 (64.2 Gbit/s) PAM4 Typ. 5.3 ps*12 (26.5625 Gbaud) Typ. 4.5 ps*12 (32.1 Gbaud) Typ. 4.1 ps*13,*14 (53.125 Gbaud) Typ. 2.5 ps*13, *14 (58.2 Gbaud)
Stressed Margin	
Stressed Eye Height	PAM4 0/1 1/2 2/3 Level, QPRBS13-CEI, Eye Height where BER is 1E–06, when using External Clock ≥32 mV*15,*16 ≥37 mV*17,*18
Stressed Eye Width	PAM4 0/1 1/2 2/3 Level, QPRBS13-CEI, Eye Width where BER is 1E–06, when using External Clock ≥7.53 ps*15,*16 ≥3.76 ps*17,*18

Termination	50Ω, GND, Variable
Termination Voltage	When set to Variable: –2.5 V to +3.5 V, 10 mV step
Connector	V connector (f)
Decision Feedback Equalizer	With a built-in Decision Feedback Equalizer (DFE)*19
Tap	1
Coefficient	Setting Range: 0 to 30, 1 step
Loss Compensation	Nom. 1.4 dB*20
Low Frequency Equalizer	With a built-in Low Frequency Equalizer *19
Gain	Setting Range: –2.0 to 0 dB, 0.5 dB step Accuracy: Typ. ±1.0 dB
Ideal Frequency Response	

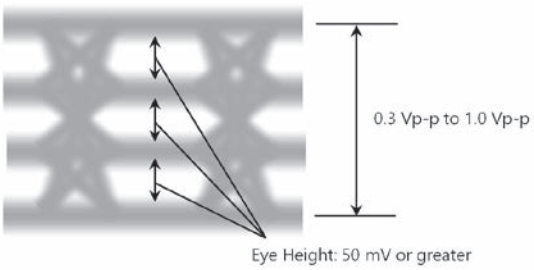
*1: Tracking is available only for NRZ.
*2: The absolute value of the difference between Data and XData Threshold values shall be 1.5 V or less.
*3: PAM4 Upper Eye and Lower Eye can be set by relative values to Middle Eye in the range of –0.4 V to +0.4 V.
*4: Single-Ended, Differential, Mark Ratio1/2, the Eye Height shall meet the specification. Example of waveform input to MU196040B when bit rate is 32.1 Gbit/s



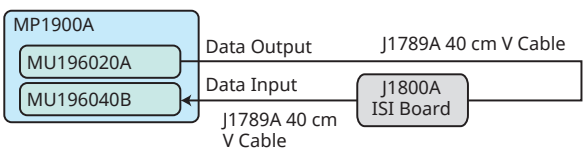
*5: Bit rate ≤32.1 Gbit/s
*6: Bit rate >32.1 Gbit/s
*7: 0/3 Level, PRBS31, Mark Ratio1/2, with connected to the MU196020A using an attenuator, with Emphasis adjusted so that the Eye Height meets the specification



Example of waveform input to MU196040B when baud rate is 32.1 Gbaud



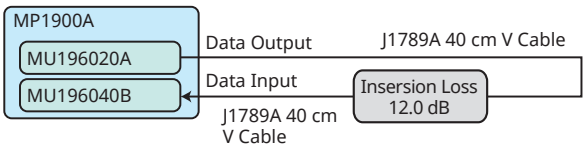
*8: Single-Ended, Differential, Baud rate ≤32.1 Gbaud
*9: Differential, Baud rate >32.1 Gbaud
*10: Data and XData can be set independently.
*11: Data and XData cannot be set independently, and can be set in the range of ±0.4 V from Middle Eye Threshold.
*12: When the Option 001, 002, or x12 is installed.
*13: When the Option 002 or x12 is installed.
*14: Value including RJ equivalent to BER 1E–12 of input signal
*15: 26.5625 Gbaud, when installed with the Option 001, 002 or x12 and the Option x11, BER 1E–12
*16: 26.5625 Gbaud, Differential, Mark Ratio1/2, when J1789A is used to connect J1800A (1 pc) and MU196020A



At a constant temperature between 20°C and 30°C, measure with a 70-GHz bandwidth sampling oscilloscope with residual jitter of less than 200 fs rms.
Adjust De-Emphasis (2 Pre Cursors and 1 Post Cursor) of MU196020A so that the product of Eye Height (1E–06) and Eye Width (1E–06) can be maximized in the differential waveform.
Calculate the 4th-order Bessel Filter (Cutoff Frequency 40 GHz) + CTLE (+1 dB Peaking at 14 GHz) and calibrate it to a PAM4 waveform with Eye Amplitude of 0.88 Vp-p (Diff) or less and Eye Linearity RLM 0.85 or more.
Activate the DFE and Low Frequency Equalizer in the MU196040B, and perform adjustment.

*17: 53.125 Gbaud, when the Option 002, x12 and x11 are installed, BER 1E–8 nom.

*18: 53.125 Gbaud, Differential, Mark Ratio1/2, when connecting a device with 12.0 dB insertion loss and MU196020A.



At a constant temperature between 20°C and 30°C, measure with a 70-GHz bandwidth sampling oscilloscope with residual jitter of less than 200 fs rms.
Adjust De-Emphasis (2 Pre Cursors and 1 Post Cursor) of MU196020A so that the product of Eye Height (1E–06) and Eye Width (1E–06) can be maximized in the differential waveform.
Calculate the 4th-order Bessel Filter (Cutoff Frequency 43 GHz) + CTLE (+1 dB Peaking at 28 GHz) and calibrate it to a PAM4 waveform with Eye Amplitude of 0.88 Vp-p (Diff) or less and Eye Linearity RLM 0.85 or more.
Activate the DFE and Low Frequency Equalizer in the MU196040B, and perform adjustment.

*19: When the Option x11 is installed.

*20: 53.125 Gbaud, Calculated from the following three:
- The BER result obtained when DFE is OFF under the condition of *18.
- The BER result obtained when DFE is OFF under the condition of *18 and 1.8 dB additional loss.
- The best BER result obtained when DFE is ON under the condition of *18 and 1.8 dB additional loss.

Clock Input

Number of Inputs	1 (Single-end)
Frequency Range	1.2 GHz to 32.1 GHz
Amplitude	0.3 Vp-p to 1.0 Vp-p (–6.5 to +4.0 dBm) (Input Frequency ≤ 16.05 GHz) 0.4 Vp-p to 1.0 Vp-p (–3.9 to +4.0 dBm) (Input Frequency > 16.05 GHz)
Termination	50Ω, AC Coupling
Connector	K (f)

Aux Input

Number of Inputs	1 (Single-end)
Variation	External Mask, Burst, Capture External Trigger
Minimum Pulse Width	1/256 of Data rate
Input Level	• 0/–1 V (H: –0.25 V to 0.05 V, L: –1.1 V to –0.8 V) • 0/–0.5 V (H: –0.05 V to 0.05 V, L: –0.55 V to –0.45 V) • Vth 0 V (Input amplitude 0.5 Vp-p to 1.0 Vp-p) Select one of the above.
Termination	GND, 50Ω
Connector	SMA (f)

Aux Output

Number of Outputs	2 (Differential)
Variation	1/n Clock (n = 8, 12, 16, 20 ... 1020, 1024), Pattern Sync, Sync Gain, Error Output
Pattern Sync	PRBS, PRGM Position: 1 to {(Least common multiple of Pattern Length' and 256) – 263}, 8 step Pattern Length' shall be the value obtained by multiplying Pattern Length setting until it becomes 1024 or more if it is 1023 or less.
Output Level	0/–0.6 V (H: –0.25 V to 0.05 V, L: –0.80 V to –0.45 V)
Termination	GND, 50Ω
Connector	SMA (f)

Pattern Detection

PRBS	
Pattern Length	$2^n - 1$ (n = 7, 9, 10, 11, 13, 15, 20, 23, 31)
Mark Ratio	1/2, 1/2INV
PRBS Generator Polynomial	n=7: $1 + X^6 + X^7$ n=9: $1 + X^5 + X^9$ n=10: $1 + X^7 + X^{10}$ n=11: $1 + X^9 + X^{11}$ n=13: $1 + X + X^2 + X^{12} + X^{13}$ n=15: $1 + X^{14} + X^{15}$ n=20: $1 + X^3 + X^{20}$ n=23: $1 + X^{18} + X^{23}$ n=31: $1 + X^{28} + X^{31}$

PRBS Inversion	This is available in PAM4 mode only. Logically inverted PRBS can be set independently for MSB and LSB.
Zero-Substitution	This is available in NRZ mode only.
Additional Bit	0 bit, 1 bit
Pattern Length	2^n or $2^n - 1$ (n = 7, 9, 10, 11, 15, 20, 23)
Start Position	Substitutes the bit coming after the maximum “0” successive bits.
Zero-Length	1 bits to (Pattern Length – 1) bits If the bit coming after Zero-substitution is “0,” then it is replaced with “1.”
Data	
Data Length	NRZ: 2 bits to 268 435 456 bits, 1 bit step PAM4: 2 to 268 435 456 symbols, 1 symbol step
Coding	NRZ, PAM4
NRZ	Normal, Invert
PAM4 Gray Coding	ON, OFF
PAM4 Precoding (1/ (1 + D)mod 4)*1	ON, OFF
PAM4 Standard Pattern	Standard-compliant PAM4-mode patterns
CEI	QPRBS13-CEI, QPRBS31-CEI
IEEE	IEEE802.3bs/cd: PRBS13Q, PRBS31Q, SSPRQ, Square Wave IEEE802.3bj: QPRBS13, JP03A, JP03B, Transmitter Linearity
RS-FEC (Option 042)	RS-FEC Scrambled Idle 50G 1 Lane (26.5625 Gbaud, 50GBASE-KR/CR/SR/FR/LR) RS-FEC Scrambled Idle 100G 1 Lane (53.125 Gbaud, 100GBASE-DR/KR1/CR1) RS-FEC-Int Scrambled Idle 100G 1 Lane (53.125 Gbaud, 100GBASE-P) RS-FEC Scrambled Idle 100G 2 Lanes (26.5625 Gbaud, 100GBASE-KR2/CR2/SR2) RS-FEC Scrambled Idle 200G 4 Lanes (26.5625 Gbaud, 200GBASE-SR4/DR4/FR4/LR4) RS-FEC Scrambled Idle 200G 2 Lanes (53.125 Gbaud, 200GBASE-KR2/CR2) RS-FEC Scrambled Idle 400G 4 Lanes (53.125 Gbaud, 400GBASE-DR4/KR4/CR4) RS-FEC Scrambled Idle 400G 8 Lanes (26.5625 Gbaud, 400GBASE-FR8/LR8)
InfiniBand	PRBS13Q (InfiniBand), PRBS23Q, PRBS31Q (InfiniBand)
Fibre Channel	PRBS31Q (Fibre Channel)
NRZ Standard Pattern	Standard-compliant NRZ-mode pattern
CEI	SSPR
RS-FEC (Option 042)	RS-FEC Scrambled Idle 25G 1 Lane (25.78125 Gbaud, 25GBASE-KR/CR/SR/LR/ER) RS-FEC Scrambled Idle 50G 2 Lanes RS (544, 514) (26.5625 Gbaud, 50GAUI-2) RS-FEC Scrambled Idle 100G 4 Lanes (25.78125 Gbaud, 100GBASE-KR4/CR4/SR4) RS-FEC Scrambled Idle 100G 4 Lanes RS (544, 514) (26.5625 Gbaud, 100GBASE-KP4)
HSSB Data*2	
Specification	PCIe1, PCIe2, PCIe3/CXL1-2, PCIe4/CXL1-2, PCIe5/CXL1-2, PCIe6/CXL3

*1: (1/(1+D) mod 4) is a generator polynomial defined in the IEEE802.3.

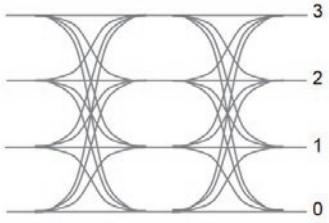
*2: Requires MU196040B-051/351

Pattern Sequence

Sequence	Repeat, Burst
Repeat	Continuous Pattern
Burst	This is available only when Coding is NRZ.
Source	Internal, External-Trigger (Aux Input), External-Enable (Aux Input)
Delay	Internal: 0 to 2 147 483 640 bits, 8 bits step Ext Trigger, Enable: 0 to 2 147 483 520 bits, 8bits step Adjust Method: Auto, Manual
Enable Period	Internal: 12 800 bits to 2 147 482 624 bits, 256 bits step Ext Trigger: 12 800 bits to 2 147 483 136 bits, 256 bits step
Burst Cycle	25 600 bits to 2 147 483 648 bits, 1024 bits step

Measurement

Counter	Error Rate (ER) Total Error Count (EC) Total Error Interval %Error Free Interval Error Rate (ER) Insertion (INS) Error Count (EC) Insertion (INS) Error Rate (ER) Omission (OMI) Error Count (EC) Omission (OMI) Frequency: 2 400.000 MHz to 64 200.000 MHz Frequency measurement accuracy: ±1 ppm ±1 kHz* Clock Count Sync. Loss Interval Clock Loss Interval Expressions enclosed in parentheses are abbreviations.
	The following are available when the Option x42 FEC Analysis is installed. Uncorrectable Codeword Error Rate (UCWER) Uncorrectable Codeword Error Count (UCWEC) Uncorrectable Codeword Error Interval Uncorrectable Codeword %Error Free Interval FEC Symbol Error Rate (ER) FEC Symbol Error Count (EC) FEC Symbol Error Interval FEC Symbol %Error Free Interval Total Codeword Count
	The following are available only for PAM4 (Diagnostics Mode ON) measurement. MSB Error Rate (ER) Total MSB Error Count (EC) Total MSB Error Rate (ER) Insertion (INS) MSB Error Count (EC) Insertion (INS) MSB Error Rate (ER) Omission (OMI) MSB Error Count (EC) Omission (OMI) LSB Error Rate (ER) Total LSB Error Count (EC) Total LSB Error Rate (ER) Insertion (INS) LSB Error Count (EC) Insertion (INS) LSB Error Rate (ER) Omission (OMI) LSB Error Count (EC) Omission (OMI) Expressions enclosed in parentheses are abbreviations.

Counter (Cont'd)	The following are available when the Option x41 SER Measurement is installed. The following are available only for PAM4 (Diagnostics Mode OFF) measurement.  Symbol Error Rate (SER) Symbol Error Count (SEC) Symbol Error Interval Symbol %Error Free Interval Details-Display1 Level 0 → 3 EC, Level 1 → 3 EC Level 0 → 2 EC, Level 1 → 2 EC Level 0 → 1 EC, Level 1 → 0 EC Level 0 → 3 ER, Level 1 → 3 ER Level 0 → 2 ER, Level 1 → 2 ER Level 0 → 1 ER, Level 1 → 0 ER Level 0 EC Total, Level 1 EC Total Level 0 ER Total, Level 1 ER Total Level 2 → 3 EC, Level 3 → 2 EC Level 2 → 1 EC, Level 3 → 1 EC Level 2 → 0 EC, Level 3 → 0 EC Level 2 → 3 ER, Level 3 → 2 ER Level 2 → 1 ER, Level 3 → 1 ER Level 2 → 0 ER, Level 3 → 0 ER Level 2 EC Total, Level 3 EC Total Level 2 ER Total, Level 3 ER Total Details-Display2 Transition 1level Level 0 → 1 and Level 1 → 0 SEC Level 1 → 2 and Level 2 → 1 SEC Level 2 → 3 and Level 3 → 2 SEC Transition 2level Level 0 → 2 and Level 2 → 0 SEC Level 1 → 3 and Level 3 → 1 SEC Transition 3level Level 0 → 3 and Level 3 → 0 SEC Upper Eye Total SEC, Middle Eye Total SEC, Lower Eye Total SEC Upper Eye Total SER, Middle Eye Total SER, Lower Eye Total SER Expressions enclosed in parentheses are abbreviations.
RS-FEC Error Distribution	Available when the Option x42 FEC Analysis is installed.
Gating	Time, Clock Count, Error Count
Gating Unit	Time: 1 second to 99 days 23 hours 59 minute 59 seconds Clock Count: >E+4 to >E+16 Error Count: >E+4 to >E+16
Cycle	Single, Repeat, Untimed
Current	ON, OFF can be set. Calculation: Progressive, Immediate Interval: 100 ms, 200 ms
Auto Sync	ON, OFF can be set. Synchronization threshold: INT, E–2 to E–8
Sync Control	PRBS: Automatic Synchronization Data: Frame On
Frame Length	NRZ: 4 bits to 64 bits, 4 bits step PAM4: 4 to 64 symbols, 4 symbol step
Frame Mask	Available
Frame Position	NRZ: 1 bits to (Pattern Length – Frame Length +1) bits, 1 bit step PAM4: 1 to (Pattern Length – Frame Length +1) symbols, 1 symbol step
Error/Alarm Condition	
Error Detection	NRZ: Insertion/Omission, Transition/Non transition PAM4: Not available
EI/EFI Interval	1 ms, 10 ms, 100 ms, 1 s

*: With a gating system and with MP1900A's reference clock (10 MHz) calibrated

Error Analysis

Block Window	Excludes the specified data pattern from measurement.
Setting Resolution	Pattern length (bits) / Step (bits) 2 to 2 097 152 / 1 2 097 153 to 4 194 304 / 2 4 194 305 to 8 388 608 / 4 8 388 609 to 16 777 216 / 8 16 777 217 to 33 554 432 / 16 33 554 433 to 67 108 864 / 32 67 108 865 to 134 217 728 / 64 134 217 729 to 268 435 456 / 128
Bit Window	Excludes any channels among internal 32 channels from measurement. (Available only in NRZ mode.)
External Mask	H: Measurement L: Mask
Capture	NRZ, PAM4 (When LSB/MSB Diagnostics is set to OFF) PAM4 is available when the Option x41 SER Measurement is installed.
Capture Mode	Sync Mode Capture: Performs error judgment. Synchronization is required between input data and pattern setting. Raw Data Capture: Does not perform error judgment. Synchronization is not required between input data and pattern setting. FEC Symbol Capture: Performs FEC Symbol error judgement. Synchronization is required between input data and pattern setting.
Number of Blocks	1, 2, 4, 8, 16, 32, 64, 128
Block Length	NRZ: 8 Mbits/n (n = Number of blocks) PAM4: 4 Msymbols/n (n = Number of blocks)
Trigger	Error Detect, Match Pattern, Manual Trigger, External Trigger (Rising Edge) Error Detect cannot be selected when Capture Mode is Raw Data Capture.
Capture Data	Displays captured results by bit or symbol sequence in NRZ or PAM4 mode. When Capture Mode is Sync Mode Capture, error bits and symbols are displayed with background color.
Error Display	NRZ: Insertion Error, Omission Error PAM4: Lower Eye Error, Middle Eye Error, Upper Eye Error, Middle/Lower Eye Error, Upper/Middle Eye Error, Upper/Middle/Lower Eye Error This is available only when Capture Mode is Sync Mode Capture.
Error Search	In PAM4 mode only, a search target can be selected from All, Upper Eye, Middle Eye and Lower Eye. Searches for continuous error bits/symbols. This is available only when Capture Mode is Sync Mode Capture.
File Save/Open	Saves the captured results and pattern to a file. Redisplays the captured results.
FEC Symbol Capture Setting	Number of FEC Symbols in a Codeword: 68, 132, 136, 272, 528, 544 FEC Symbols Bit Length in a FEC Symbol: 10, 20 bits FEC Symbol Error Threshold: 1 to 32 FEC Symbols/step 1
Error Mapping	Visually maps errors using bits with colored-background in NRZ or PAM4 mode. This is available only when Capture Mode is Sync Mode Capture.
Error Display	NRZ: Insertion Error, Omission Error PAM4: Lower Eye Error, Middle Eye Error, Upper Eye Error, Middle/Lower Eye Error, Upper/Middle Eye Error, Upper/Middle/Lower Eye Error
File Open	Remaps the captured results (errors).

Auto Measurement

Auto Adjust	NRZ: Vth direction only (Phase direction not supported.)*1 PAM4: MSB Vth direction only (Phase direction not supported.)*1, *2
Auto Search	NRZ: Available*1 PAM4 (LSB/MSB Diagnostics ON/OFF): Available*1, *3
BER/SER Logging	NRZ: With BER Logging PAM4: With SER Logging

*1: PRBS Pattern, Mark Ratio 1/2
*2: Each of amplitudes shall be equal.
*3: Each of 0/1, 1/2 and 2/3 levels is equal.

Variable Clock Delay

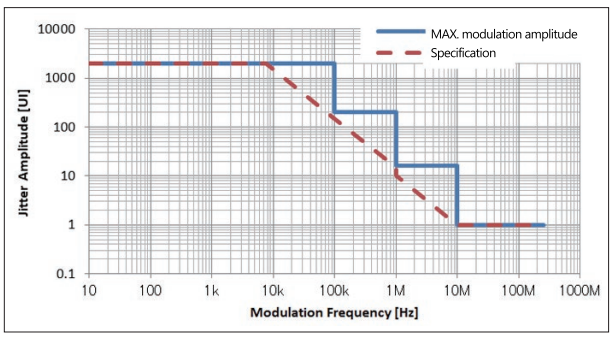
Phase Variable Range	–1000 mUI to +1000 mUI, 2 mUI step
Accuracy	±50 mUIp-p* (Baud rate ≤32.1 Gbaud, Typical value) ±100 mUIp-p* (Baud rate >32.1 Gbaud, Typical value)
mUI-ps Switching	Available (internally converted into ps)
Calibration	Available (when jitter modulation is off)
Calibration Indicator	This indicator is on when Calibration is required due to: • Change in 1/1Clock frequency by ±250 kHz. • Change in the ambient temperature by ±5°C.

*: Measure using an oscilloscope with residual jitter of less than 200 fs rms.

Jitter Tolerance

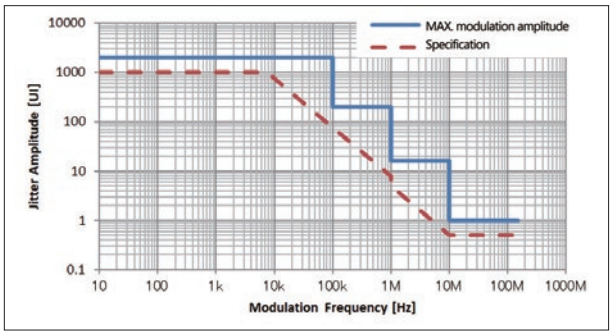
Jitter Tolerance	
For NRZ Input	Bit rate: 32.1 Gbit/s, 64.2 Gbit/s* Pattern: PRBS2^{31} – 1 32.1 Gbits: With MU181500B, SSC with frequency of 33 kHz and deviation of 5300 ppm can be applied simultaneously with RJ with amplitude of 0.3 UI. 64.2 Gbits: With MU181500B, SSC with frequency of 33 kHz and deviation of 3300 ppm can be applied simultaneously with RJ with amplitude of 0.3 UI. These specifications are defined assuming the following conditions: Loopback connection to the MU196020A, at a constant temperature between 20°C and 30°C. When RJ+BUJ is bigger than 0.5 UIp-p or SJ + RJ + BUJ is bigger than the standard value + 0.3 UIp-p, "Overload" is displayed on the MU181500B screen.

32.1 Gbit/s



Modulation Frequency [Hz]	Max. Modulation Amplitude [UIp-p]	Specification [UIp-p]
10	2,000	2,000
7,500	2,000	2,000
100,000	2,000	150
1,000,000	200	15
10,000,000	16	1
150,000,000	1	1

64.2 Gbit/s

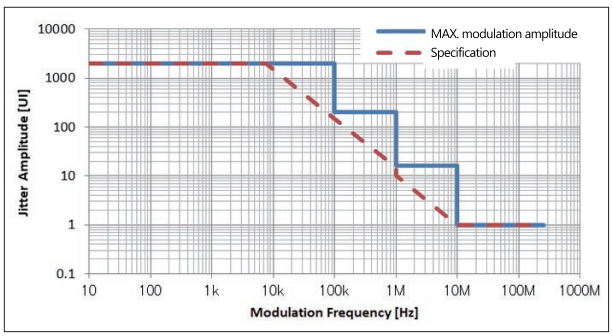


Modulation Frequency [Hz]	Max. Modulation Amplitude [UIp-p]	Specification [UIp-p]
10	2,000	1,000
7,500	2,000	1,000
100,000	2,000	75
1,000,000	200	8
10,000,000	16	0.5
150,000,000	1	0.5

PAM4 ED MU196040B Specifications

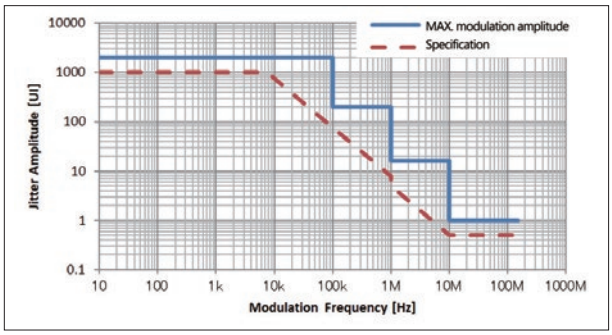
For PAM4 Input	Baud rate: 32.1 Gbaud, 58.2 Gbaud* Pattern: PRBS31Q 32.1 Gbaud: With MU181500B, SSC with frequency of 33 kHz and deviation of 5300 ppm can be applied simultaneously with RJ with amplitude of 0.3 UI. 58.2 Gbaud: With MU181500B, SSC with frequency of 33 kHz and deviation of 3300 ppm can be applied simultaneously with RJ with amplitude of 0.3 UI. These specifications are defined assuming the following conditions: Loopback connection to the MU196020A, at a constant temperature between 20°C and 30°C. When RJ+BUJ is bigger than 0.5 UIp-p or SJ + RJ + BUJ is bigger than the standard value + 0.3 UIp-p, "Overload" is displayed on the MU181500B screen.

32.1 Gbaud



Modulation Frequency [Hz]	Max. Modulation Amplitude [UIp-p]	Specification [UIp-p]
10	2,000	2,000
7,500	2,000	2,000
100,000	2,000	150
1,000,000	200	15
10,000,000	16	1
150,000,000	1	1

58.2 Gbaud



Modulation Frequency [Hz]	Max. Modulation Amplitude [UIp-p]	Specification [UIp-p]
10	2,000	1,000
7,500	2,000	1,000
100,000	2,000	75
1,000,000	200	8
10,000,000	16	0.5
150,000,000	1	0.5

*: When the Option 002 or x12 is installed.

Clock Recovery

Operating Bit Rate*1	When the Option x21 is installed. NRZ: 2.4 Gbit/s to 29.0 Gbit/s PAM4: 2.4 Gbaud to 29.0 Gbaud When the Option x22, or x21 + x24 is installed. NRZ: 2.4 Gbit/s to 32.1 Gbit/s PAM4: 2.4 Gbaud to 32.1 Gbaud When the Option x23 is installed. NRZ: 51.0 Gbit/s to 58.2 Gbit/s PAM4: 51.0 Gbaud to 58.2 Gbaud
Setting Range*2	When the Option x21 is installed. NRZ: 2.400 000 Gbit/s to 29.000 000 Gbit/s, 0.000 001 Gbit/s step PAM4: 2.400 000 Gbaud to 29.000 000 Gbaud, 0.000 001 Gbaud step When the Option x22, or x21 + x24 is installed. NRZ: 2.400 000 Gbit/s to 32.100 000 Gbit/s, 0.000 001 Gbit/s step PAM4: 2.400 000 Gbaud to 32.100 000 Gbaud, 0.000 001 Gbaud step When the Option x23 is installed. NRZ: 51.000 000 Gbit/s to 58.200 000 Gbit/s, 0.000 001 Gbit/s step PAM4: 51.000 000 Gbaud to 58.200 000 Gbaud, 0.000 001 Gbaud step

PAM4 ED MU196040B Specifications

<table>
<tr><td>Supported Standard and Bit Rate</td><td>For NRZ mode
<table>
<tr><th>Standard</th><th>Bit Rate [Gbit/s]</th></tr>
<tr><td>CEI-56G*3</td><td>56.000 000</td></tr>
<tr><td>100G ULH*4</td><td>32.100 000</td></tr>
<tr><td>32G FC*5</td><td>28.050 000</td></tr>
<tr><td>CEI-28G*5</td><td>28.000 000</td></tr>
<tr><td>100G OTU4*5</td><td>27.952 496</td></tr>
<tr><td>100 GbE(25.78 × 4)*5</td><td>25.781 250</td></tr>
<tr><td>InfiniBand EDR*5</td><td>25.781 250</td></tr>
<tr><td>InfiniBand FDR*5</td><td>14.062 500</td></tr>
<tr><td>16G FC*5</td><td>14.025 000</td></tr>
<tr><td>10G FC Over FEC*5</td><td>11.316 800</td></tr>
<tr><td>10 GbE Over FEC*5</td><td>11.095 700</td></tr>
<tr><td>OTU2*5</td><td>10.709 225</td></tr>
<tr><td>G975 FEC*5</td><td>10.664 228</td></tr>
<tr><td>10G FC*5</td><td>10.518 750</td></tr>
<tr><td>10 GbE*5</td><td>10.312 500</td></tr>
<tr><td>InfiniBand QDR*5</td><td>10.000 000</td></tr>
<tr><td>OC-192/STM-64*5</td><td>9.953 280</td></tr>
<tr><td>8G FC*5</td><td>8.500 000</td></tr>
<tr><td>HSBI*5</td><td>6.250 000</td></tr>
<tr><td>InfiniBand DDR*5</td><td>5.000 000</td></tr>
<tr><td>4G FC*5</td><td>4.250 000</td></tr>
<tr><td>XAUI*5</td><td>3.125 000</td></tr>
<tr><td>OTU1*5</td><td>2.666 060</td></tr>
<tr><td>InfiniBand SDR*5</td><td>2.500 000</td></tr>
<tr><td>OC-48/STM-16*5</td><td>2.488 320</td></tr>
</table>
For PAM4 mode
<table>
<tr><th>Standard</th><th>Bit Rate [Gbaud]</th></tr>
<tr><td>CEI 112G*3</td><td>56.000 000</td></tr>
<tr><td>400 GbE (53.1 × 4)*3</td><td>53.125 000</td></tr>
<tr><td>64G FC*5</td><td>28.900 000</td></tr>
<tr><td>CEI 56G*5</td><td>28.000 000</td></tr>
<tr><td>200 GbE (26.6 × 4)*5</td><td>26.562 500</td></tr>
<tr><td>InfiniBand HDR*5</td><td>26.562 500</td></tr>
</table></td></tr>
<tr><td>Operating Bit Rate Tracking</td><td>Tracks the operating baud rate of the PPG selected from the PPGs installed in the same MP1900A.
It is provided with an indicator that turns on when the PPG's operating baud rate is out of the tracking range.</td></tr>
<tr><td>Maximum Number of Consecutive Zeros*2</td><td>When the Option x21, x22, or x21 + x24 is installed.
72 bit
Zero Substitution 2^{15},
Target loop band: 1/1667, 1/2578 at 2.4G to 25.499 999G,
1/1667, 1/2578, 1/6640 at 25.5G to 32.1G
When the Option x23 is installed.
72 bit
Zero Substitution 2^{15},
Target loop band: 1/6640, 1/13280 at 51.0G to 58.2G</td></tr>
<tr><td>Lock Range*2</td><td>When the Option x21, x22, or x21 + x24 is installed.
±200 ppm
2.4G to 25.499 999G, The target loop band is specified by 1/1667, 1/2578.
±100 ppm
25.5G to 32.1G, The target loop band is specified by 1/1667, 1/2578, 1/6640.
When the Option x23 is installed.
±100 ppm
51.0 to 58.2 G, The target loop band is specified by 1/6640, 1/13280.</td></tr>
</table>

Target Loop Band*3

When the Option x21, x22, or x21 + x24 is installed.

25.5G to 32.1G*6

Baud rate/1667
Baud rate/2578
Baud rate/6640
Jitter Tolerance

2.4G to 25.499 999G

Baud rate/1667
Baud rate/2578
Jitter Tolerance
Variable

When Variable is selected, the ranges are as follows:

Baud Rate [Gbaud]	Range [MHz]	Step [MHz]
2.400 000 to 5.500 000	3	—
5.500 001 to 7.500 000	3 to 4	1
7.500 001 to 9.500 000	3 to 5	1
9.500 001 to 10.500 000	3 to 6	1
10.500 001 to 12.500 000	3 to 7	1
12.500 001 to 14.500 000	3 to 8	1
14.500 001 to 15.500 000	3 to 9	1
15.500 001 to 17.500 000	3 to 10	1
17.500 001 to 19.500 000	3 to 11	1
19.500 001 to 20.500 000	3 to 12	1
20.500 001 to 22.500 000	3 to 13	1
22.500 001 to 24.500 000	3 to 14	1
24.500 001 to 25.499 999	3 to 15	1

When the Option x23 is installed.

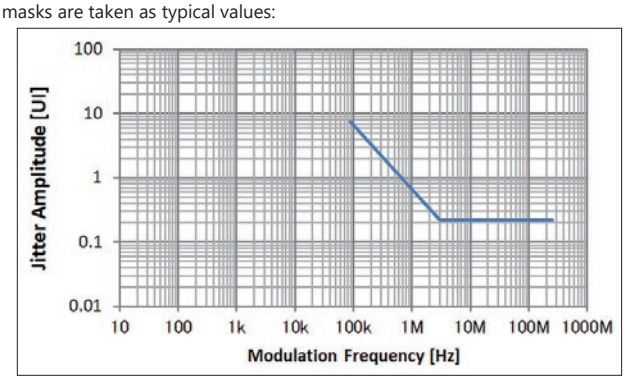
51.0G to 58.2G*7

Baud rate/6640
Baud rate/13280
Jitter Tolerance

Jitter Tolerance*8

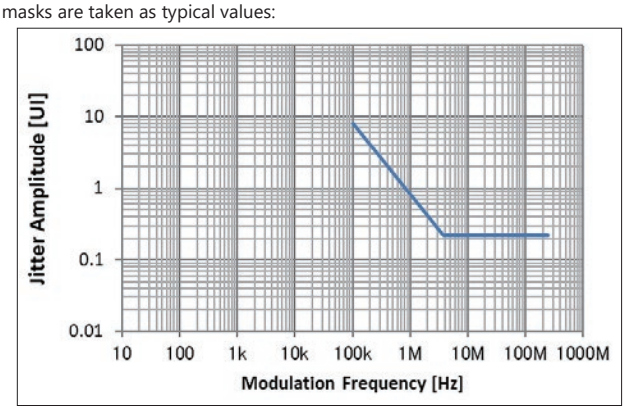
NRZ Input

At the bit rate of 58.0 Gbit/s, conforming to Jitter Tolerance Mask defined by the "CEI 56G Jitter Tolerance Mask". The following masks are taken as typical values:



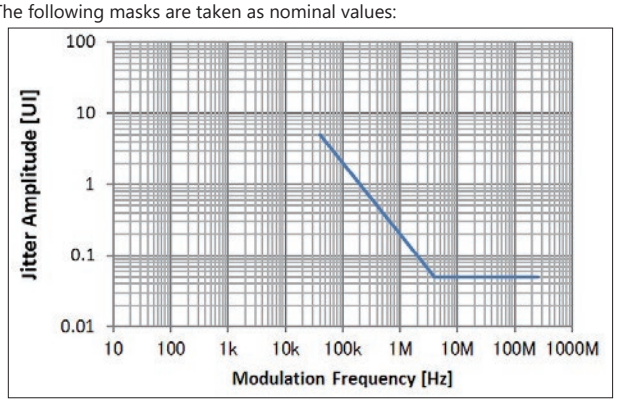
Modulation Frequency [Hz]	Jitter Tolerance Mask [UIp-p]
87,349	7.5
2,977,820	0.22
250,000,000	0.22

At the bit rate of 28.05 Gbit/s, conforming to Jitter Tolerance Mask defined by the "32G FC Jitter Tolerance Mask". The following masks are taken as typical values:



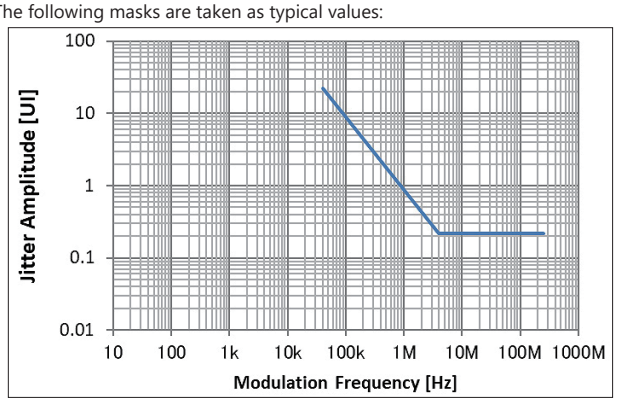
Modulation Frequency [Hz]	Jitter Tolerance Mask [UIp-p]
100,000	8.16
3,709,271	0.22
250,000,000	0.22

PAM4 Input	At the bit rate of 53.125 Gbaud, conforming to Jitter Tolerance Mask defined by the "CEI-112G-VSR Jitter Tolerance Mask". The following masks are taken as nominal values:



Modulation Frequency [Hz]	Jitter Tolerance Mask [UIp-p]
40,004	5
4,000,377	0.05
250,000,000	0.05

At the bit rate of 26.5625 Gbaud, conforming to Jitter Tolerance Mask defined by the "IEEE802.3bs Jitter Tolerance Mask".
The following masks are taken as typical values:



Modulation Frequency [Hz]	Jitter Tolerance Mask [UIp-p]
40,000	22
4,000,000	0.22
250,000,000	0.22

*1: When the Option x21, x22, x23, or x24 is installed.
These are specified with the conditions of PRBS Pattern and Mark Ratio 1/2 (in PAM4 mode, MSB Mark Ratio 1/2) unless otherwise specified.
*2: When the ED is tracking the PPG linked with MU181000A/B and MU181500B, it operates in the same ranges of bit rate and baud rate as the PPG if a recovered clock is used as a system clock.
*3: When the Option x23 is installed.
*4: When the Option x22, or x21 + x24 is installed.
*5: When the Option x21, x22, or x21 + x24 is installed.
*6: The SSPRQ pattern supports Baud rate/6640 only. When set to Jitter Tolerance, Baud rate/1667 or higher.
*7: The SSPRQ pattern supports Baud rate/6640 only. When set to Jitter Tolerance, Baud rate/6640 or higher.
*8: Specified at a constant temperature between +20° and +30°C.

General

Dimensions and Mass	234 (W) × 21 (H) × 175 (D) mm (Protrusions excluded), 2.5 kg max.
Operating Temperature	+15°C to +30°C MP1900A's ambient temperature. MU196040B shall operate when installed.
Storage Temperature	–20°C to +60°C MU196040B installed to MP1900A shall comply with MIL-T-28800E Class 5.

PAM4 ED MU196040A Specifications

Operating Baud Rate

Operating Baud Rate	2.4 Gbaud to 32.1 Gbaud

System Clock

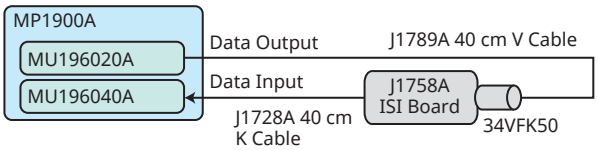
System Clock	External, Recovered Clock (When the Option x22 is installed)

Data Input

Number of Inputs	2 (Data, XData) (Differential)
Input Condition	Single-end, Differential 50Ω, Differential 100Ω When set to Differential 50Ω or Differential 100Ω: Independent, Tracking, Alternate*1 When set to Alternate: Data-XData, XData-Data*2 When set to Single-end: Data, XData*3
Signal Type	NRZ, PAM4
LSB/MSB Diagnostics	When set to PAM4, the PAM4 mode can be switched between as follows: Diagnostics Mode OFF: Treats signals as symbols by receiving LSB and MSB while synchronizing them with each other. Diagnostics Mode ON: Asynchronously receives LSB and MSB.
Input Amplitude	NRZ: The range in which the Auto Adjust function operates. PAM4: The range in which the Auto Search PAM4 Fine function operates. NRZ: 0.05 Vp-p to 1.0 Vp-p*4 PAM4: 0.3 Vp-p to 1.0 Vp-p*5
Threshold Voltage	NRZ, PAM4 Middle Eye Threshold: –3.5 V to +3.3 V, 1 mV step*2, *6 PAM4 Upper Eye Threshold: –3.9 V to +3.7 V, 1 mV step*7 PAM4 Lower Eye Threshold: –3.9 V to +3.7 V, 1 mV step*7
Input Sensitivity	Single-end, Mark Ratio1/2, when connecting directly to the MU196020A with J1789A. When the Option 001 is installed, 34VKF50 shall be included. At a constant temperature between 20°C and 30°C
Eye Amplitude	NRZ, PRBS31 Typ. 32 mVp-p, ≤ 50 mVp-p*8
Eye Height	NRZ, PRBS31 Typ. 23 mV*8 PAM4 Typ. 23 mV, ≤ 50 mV*9
Phase Margin	When connecting directly to the MU196020A with J1789A. When the Option 001 is installed, 34VKF50 shall be included. At a constant temperature between 20°C and 30°C, when using External Clock NRZ, PRBS31, Differential, Mark Ratio 1/2, when inputting 1.0 Vp-p Typ. 25.8 ps*10 Typ. 18.0 ps*11 PAM4 0/3 Level, Eye Width where BER is 1E–06, PRBS31, Single-end, Mark Ratio1/2, when inputting 0.5 Vp-p, Emphasis ON (Best values in the range of 1Pre ≤ 5 dB and 1Post ≤ 5 dB) Typ. 5.3 ps*12 Typ. 4.5 ps*13
Stressed Margin*14	
Stressed Eye Height	PAM4 0/1 1/2 2/3 Level, QPRBS13-CEI, Eye Height where BER is 1E–06, when using External Clock ≥32 mV*15
Stressed Eye Width	PAM4 0/1 1/2 2/3 Level, QPRBS13-CEI, Eye Width where BER is 1E–06, when using External Clock ≥7.15 ps*15
Termination	50Ω, GND, Variable
Termination Voltage	When set to Variable: –2.5 V to +3.5 V, 10 mV step
Connector	K (f) (When the Option 001 is installed)

*1: Tracking is available only for NRZ.
*2: The absolute value of the difference between Data and XData Threshold values shall be 1.5 V or less.
*3: PAM4 Upper Eye and Lower Eye can be set by relative values to Middle Eye in the range of –0.4 V to +0.4 V.
*4: Single-end, Differential
*5: 0/3 Level, PRBS31, Single-end, Differential, when connecting directly to the MU196020A.
*6: Data and XData can be set independently.
*7: Data and XData cannot be set independently, and can be set in the range of ±0.4 V from Middle Eye Threshold.
*8: 26.5625 Gbit/s, 32.1 Gbit/s, when the Option 001 is installed.
*9: 26.5625 Gbaud, 32.1 Gbaud, when the Option 001 is installed.
*10: 26.5625 Gbit/s, when the Option 001 is installed.
*11: 32.1 Gbit/s, when the Option 001 is installed.
*12: 26.5625 Gbaud, when the Option 001 is installed.
*13: 32.1 Gbaud, when the Option 001 is installed.

*14: Differential, Mark Ratio1/2, when connecting J1758A and MU196020A by using J1789A, 34VKF50 and J1728A.



At a constant temperature between 20°C and 30°C, measure with a 70-GHz bandwidth sampling oscilloscope with residual jitter of less than 200 fs rms.
Adjust MU196020A De-Emphasis (2 Pre Cursors and 1 Post Cursor) so that the product of Eye Height (1E–06) and Eye Width (1E–06) can be maximized in the differential waveform.
Calculate the 4th Bessel Filter (Cutoff Frequency 50 GHz) + CTLE (+1 dB Peaking at 14 GHz) and calibrate it to a PAM4 waveform with Eye Amplitude of 0.88 Vp-p (Diff) or less and Eye Linearity RLM 0.85 or more.

*15: 28 Gbaud, when the Option 001 is installed, BER 1E–12

Clock Input

Number of Inputs	1 (Single-end)
Frequency Range	2.4 GHz to 32.1 GHz
Amplitude	0.3 Vp-p to 1.0 Vp-p (–6.5 to +4.0 dBm) (Input Frequency ≤ 16.05 GHz) 0.4 Vp-p to 1.0 Vp-p (–3.9 to +4.0 dBm) (Input Frequency > 16.05 GHz)
Termination	50Ω, AC Coupling
Connector	K (f)

Aux Input

Number of Inputs	1 (Single-end)
Variation	External Mask, Burst
Minimum Pulse Width	1/256 of Data rate
Input Level	• 0/–1 V (H: –0.25 V to 0.05 V, L: –1.1 V to –0.8 V) • 0/–0.5 V (H: –0.05 V to 0.05 V, L: –0.55 V to –0.45 V) • Vth 0 V (Input amplitude 0.5 Vp-p to 1.0 Vp-p) Select one of the above.
Termination	GND, 50Ω
Connector	SMA (f)

Aux Output

Number of Outputs	2 (Differential)
Variation	1/n Clock (n = 8, 12, 16, 20 ... 1020, 1024), Pattern Sync, Sync Gain, Error Output
Pattern Sync	PRBS, PRGM Position: 1 to {(Least common multiple of Pattern Length' and 128) –135}, 8 step (When the Option 001 is installed) Pattern Length' shall be the value obtained by multiplying Pattern Length setting until it becomes 1024 or more if it is 1023 or less.
Output Level	0/–0.6 V (H: –0.25 V to 0.05 V, L: –0.80 V to –0.45 V)
Termination	GND, 50Ω
Connector	SMA (f)

Pattern Detection

PRBS	
Pattern Length	$2^n - 1$ (n = 7, 9, 10, 11, 13, 15, 20, 23, 31)
Mark Ratio	1/2, 1/2INV
PRBS Generator Polynomial	n=7: $1 + X^6 + X^7$ n=9: $1 + X^5 + X^9$ n=10: $1 + X^7 + X^{10}$ n=11: $1 + X^9 + X^{11}$ n=13: $1 + X + X^2 + X^{12} + X^{13}$ n=15: $1 + X^{14} + X^{15}$ n=20: $1 + X^3 + X^{20}$ n=23: $1 + X^{18} + X^{23}$ n=31: $1 + X^{28} + X^{31}$
PRBS Inversion	This is available in PAM4 mode only. Logically inverted PRBS can be set independently for MSB and LSB.
Zero-Substitution	This is available in NRZ mode only.
Additional Bit	0 bit, 1 bit
Pattern Length	2^n or $2^n - 1$ (n = 7, 9, 10, 11, 15, 20, 23)
Start Position	Substitutes the bit coming after the maximum "0" successive bits.
Zero-Length	1 bits to (Pattern Length – 1) bits If the bit coming after Zero-substitution is "0," then it is replaced with "1."

Data	
Data Length	NRZ: 2 bits to 268 435 456bits, 1 bit step PAM4: 2 to 268 435 456 symbol, 1 symbol step
Coding	NRZ, PAM4
NRZ	Normal, Invert
PAM4 Gray Coding	ON, OFF
PAM4 Precoding (1/ (1 + D)mod 4)*	ON, OFF
PAM4 Standard Pattern	Standard-compliant PAM4-mode patterns
CEI	QPRBS13-CEI, QPRBS31-CEI
IEEE	IEEE802.3bs/cd: PRBS13Q, PRBS31Q, SSPRQ, Square Wave IEEE802.3bj: QPRBS13, JP03A, JP03B, Transmitter Linearity
InfiniBand	PRBS13Q (InfiniBand), PRBS23Q, PRBS31Q (InfiniBand)
Fibre Channel	PRBS31Q (Fibre Channel)
NRZ Standard Pattern	Standard-compliant NRZ-mode pattern
CEI	SSPR

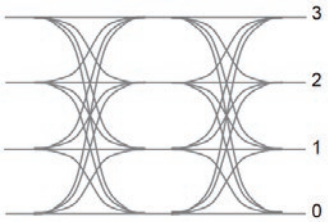
*: (1/(1+D) mod 4) is a generator polynomial defined in the IEEE802.3.

Pattern Sequence

Sequence	Repeat, Burst
Repeat	Continuous Pattern
Burst	This is available only when Coding is NRZ.
Source	Internal, External-Trigger (Aux Input), External-Enable (Aux Input)
Delay	Internal: 0 to 2 147 483 640 bits, 8 bits step Ext Trigger, Enable: 0 to 2 147 483 520 bits, 8bits step Adjust Method: Auto, Manual
Enable Period	Internal: 12800 bits to 2 147 482 624 bits, 256 bits step Ext Trigger: 12800 bits to 2 147 483 136 bits, 256 bits step
Burst Cycle	25600 bits to 2 147 483 648 bits, 1024 bits step

Measurement

Counter	Error Rate (ER) Total Error Count (EC) Total Error Interval %Error Free Interval Error Rate (ER) Insertion (INS) Error Count (EC) Insertion (INS) Error Rate (ER) Omission (OMI) Error Count (EC) Omission (OMI) Frequency: 2 400.000 MHz to 32 100.000 MHz Frequency measurement accuracy: ±1 ppm ±1 kHz* Clock Count Sync. Loss Interval Clock Loss Interval Expressions enclosed in parentheses are abbreviations.
	The following are available only for PAM4 (Diagnostics Mode ON) measurement. MSB Error Rate (ER) Total MSB Error Count (EC) Total MSB Error Rate (ER) Insertion (INS) MSB Error Count (EC) Insertion (INS) MSB Error Rate (ER) Omission (OMI) MSB Error Count (EC) Omission (OMI) LSB Error Rate (ER) Total LSB Error Count (EC) Total LSB Error Rate (ER) Insertion (INS) LSB Error Count (EC) Insertion (INS) LSB Error Rate (ER) Omission (OMI) LSB Error Count (EC) Omission (OMI) Expressions enclosed in parentheses are abbreviations.

Counter (Cont'd)	The following are available when the Option x41 SER Measurement is installed. The following are available only for PAM4 (Diagnostics Mode OFF) measurement.  Symbol Error Rate (SER) Symbol Error Count (SEC) Symbol Error Interval Symbol %Error Free Interval Level 0 → 3 EC, Level 1 → 3 EC Level 0 → 2 EC, Level 1 → 2 EC Level 0 → 1 EC, Level 1 → 0 EC Level 0 → 3 ER, Level 1 → 3 ER Level 0 → 2 ER, Level 1 → 2 ER Level 0 → 1 ER, Level 1 → 0 ER Level 0 EC Total, Level 1 EC Total Level 0 ER Total, Level 1 ER Total Level 2 → 3 EC, Level 3 → 2 EC Level 2 → 1 EC, Level 3 → 1 EC Level 2 → 0 EC, Level 3 → 0 EC Level 2 → 3 ER, Level 3 → 2 ER Level 2 → 1 ER, Level 3 → 1 ER Level 2 → 0 ER, Level 3 → 0 ER Level 2 EC Total, Level 3 EC Total Level 2 ER Total, Level 3 ER Total Expressions enclosed in parentheses are abbreviations.
Gating	Time, Clock Count, Error Count
Gating Unit	Time: 1 second to 99 days 23 hours 59 minute 59 seconds Clock Count: >E+4 to >E+16 Error Count: >E+4 to >E+16
Cycle	Single, Repeat, Untimed
Current	ON, OFF can be set. Calculation: Progressive, Immediate Interval: 100 ms, 200 ms
Auto Sync	ON, OFF can be set. Synchronization threshold: INT, E–2 to E–8
Sync Control	PRBS: Automatic Synchronization Data: Frame On
Frame Length	NRZ: 4 bits to 64 bits, 4 bits step PAM4: 4 to 64 symbols, 4 symbol step
Frame Mask	Available
Frame Position	NRZ: 1 bits to (Pattern Length – Frame Length +1) bits, 1 bit step PAM4: 1 to (Pattern Length – Frame Length +1) symbols, 1 symbol step
Error/Alarm Condition	
Error Detection	NRZ: Insertion/Omission, Transition/Non transition PAM4: Not available
EI/EFI Interval	1 ms, 10 ms, 100 ms, 1 s

*: With a gating system and with MP1900A's reference clock (10 MHz) calibrated

Error Analysis

Block Window	Excludes the specified data pattern from measurement.
Setting Resolution	Pattern length (bits) — Step (bits) 2 to 2 097 152 — 1 2 097 153 to 4 194 304 — 2 4 194 305 to 8 388 608 — 4 8 388 609 to 16 777 216 — 8 16 777 217 to 33 554 432 — 16 33 554 433 to 67 108 864 — 32 67 108 865 to 134 217 728 — 64 134 217 729 to 268 435 456 — 128
Bit Window	Excludes any channels among internal 32 channels from measurement. (Available only in NRZ mode.)
External Mask	H: Measurement L: Mask

PAM4 ED MU196040A Specifications

Auto Measurement

Auto Adjust	NRZ: Vth direction only (Phase direction not supported.)*1 PAM4: MSB Vth direction only (Phase direction not supported.)*1, *2
Auto Search	NRZ: Available*1 PAM4 (LSB/MSB Diagnostics ON/OFF): Available*1, *2

*1: PRBS Pattern, Mark Ratio 1/2
*2: Each of amplitudes shall be equal.

Variable Clock Delay

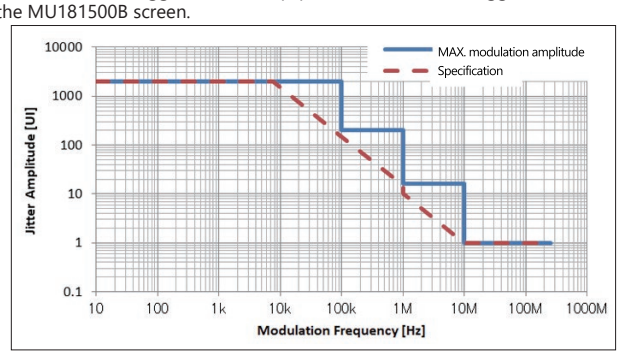
Phase Variable Range	–1000 mUI to +1000 mUI, 2 mUI step
Accuracy	Typ. ±50 mUIp-p*
mUI-ps Switching	Available (internally converted into ps)
Calibration	Available (when jitter modulation is off)
Calibration Indicator	This indicator is on when Calibration is required due to: • Change in 1/1Clock frequency by ±250 kHz. • Change in the ambient temperature by ±5°C.

*: Measure using an oscilloscope with residual jitter of less than 200 fs rms.

Jitter Tolerance

Jitter Tolerance

For NRZ output
Bit rate: 32.1 Gbit/s
Pattern: PRBS2^{31} – 1
With MU181500B, SSC with frequency of 33 kHz and deviation of 5300 ppm can be applied simultaneously with RJ with amplitude of 0.3 UI.
These specifications are defined assuming the following conditions:
Loopback connection to the MU196020A, at a constant temperature between 20°C and 30°C.
When RJ+BUJ is bigger than 0.5 UIp-p or SJ + RJ + BUJ is bigger than the standard value + 0.3 UIp-p, "Overload" is displayed on the MU181500B screen.



Modulation Frequency [Hz]	Max. Modulation Amplitude [UIp-p]	Specification [UIp-p]
10	2,000	2,000
7,500	2,000	2,000
100,000	2,000	150
1,000,000	200	15
10,000,000	16	1
250,000,000	1	1

Clock Recovery

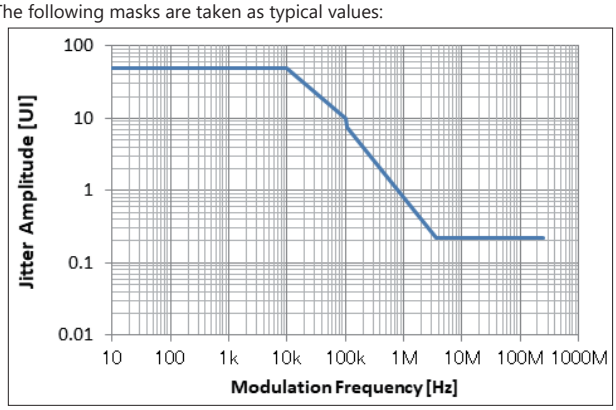
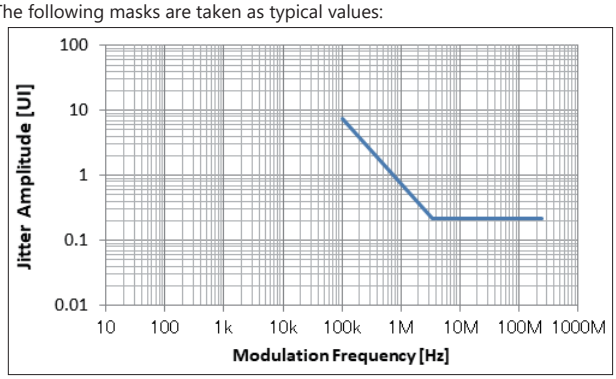
Operating Bit Rate	NRZ: 25.5 Gbit/s to 32.1 Gbit/s PAM4: 25.5 to 32.1 Gbaud
Setting Range	25.500 000 to 32.100 000 Gbaud, 0.000 001 Gbaud step
Supported Standard and Bit Rate	For NRZ mode

Standard	Bit Rate [Gbit/s]
100G ULH	32.100 000
32G FC	28.050 000
CEI-28G	28.000 000
100G OTU4	27.952 496
100GbE (25.78 × 4)	25.781 250
InfiniBand EDR	25.781 250

For PAM4 mode

Standard	Bit Rate [Gbaud]
64G FC	28.900 000
CEI-56G	28.000 000
200GbE (26.6 × 4)	26.562 500
InfiniBand HDR	26.562 500

Operating Bit Rate Tracking	Tracks the operating bit rate of the PPG selected from the PPGs installed in the same MP1900A.
Maximum Number of Consecutive Zeros*2	72 bit (Zero Substitution 2^{15})
Lock Range*2	±100 ppm
Target Loop Band*3	$\frac{\text{Baud rate}}{1667}$ MHz, $\frac{\text{Baud rate}}{2578}$ MHz, $\frac{\text{Baud rate}}{6640}$ MHz, Jitter Tolerance

Jitter Tolerance Clock Recovery*4, *5	At the bit rate of 28.05 Gbaud, conforming to Jitter Tolerance Mask defined by the "32G FC standard". The following masks are taken as typical values:  Modulation Frequency [Hz] / Jitter Tolerance Mask [UIp-p] 10 / 50 10,000 / 50 100,000 / 10 108,805 / 7.5 3,709,271 / 0.22 250,000,000 / 0.22 At the bit rate of 25.78125 Gbaud, conforming to Jitter Tolerance Mask defined by the "100 GbE (25.78G × 4) standard". The following masks are taken as typical values:  Modulation Frequency [Hz] / Jitter Tolerance Mask [UIp-p] 100,000 / 7.5 3,409,256 / 0.22 250,000,000 / 0.22

*1: When the Option x22 is installed, these are specified with the conditions of PRBS Pattern and Mark Ratio 1/2 (in PAM4 mode, MSB Mark Ratio 1/2) unless otherwise specified.
*2: The target loop band is specified by 1/1667, 1/2578, 1/6640.
*3: The SSPRQ pattern supports Baud rate/6640 only. When set to Jitter Tolerance, Baud rate/1667 or higher.
*4: Defined assuming the following conditions: Loop-back connection to MU196020A, NRZ input, Test Pattern (Length): PRBS 2^{31}–1, Data input amplitude: 0.1 Vp-p
*5: Typical value, specified at a constant temperature between 20°C and 30°C.

General

Dimensions and Mass	234 (W) × 21 (H) × 175 (D) mm (Protrusions excluded), 2.5 kg max.
Operating Temperature	+15°C to +30°C MP1900A's ambient temperature. MU196040A shall operate when installed.
Storage Temperature	–20°C to +60°C MU196040A installed to MP1900A shall comply with MIL-T-28800E Class 5.

Noise Generator MU196050B Specifications

Data Output

Noise Output	
Number of Channels	1
Number of Inputs per Channel	2 (Differential)
Termination	50Ω, AC Coupling
Connector	SMA (J)

Differential Mode Interface (DMI)*

Amplitude	0 to 200 mVp-p (Differential) (Defined when CMI ON, 0 mV, and 120 MHz are set)
Amplitude Setting Step	0.1 mV
Amplitude Accuracy	±20% ±10 mV (Defined at a temperature between 20°C and 30°C)
Frequency	2 GHz to 10 GHz
Frequency Setting Step	10 MHz
Waveform	Sinusoidal wave
Presets	PCIe 3, PCIe 4, PCIe 5, PCIe 6, PCIe 7
Output control	ON and OFF can be selected. (Either DMI/CMI or External Input can be selected.) (DMI/CMI can be output simultaneously.)

*: Connect a Coaxial Cable J1948A (0.4 m, SMA connector) and a Pick-off Tee J1793A (pick-off path) to the Noise Output, and define the measurement point at the end of the connection where a 34VKF50A and a Coaxial Cable J1821A (0.8 m, K connector) are connected to the OUT terminal of the J1793A.
⚠ Always use in combination with the Pick OFF Tee J1793A standard accessory.

Common Mode Interface (CMI)*

Amplitude	0 to 250 mVp-p (Single-ended) (Defined when DMI ON, 0 mV, and 2.1 GHz are set)
Amplitude Setting Step	2 mV
Amplitude Accuracy	±20% ±25 mV (Defined at a temperature between 20°C and 30°C)
Frequency	Low Band: 100 MHz to 1 GHz High Band: 1 GHz to 6 GHz
Frequency Setting Step	Low Band: 1 MHz High Band: 10 MHz
Waveform	Sinusoidal wave
Output Control	ON and OFF can be selected. (Either DMI/CMI or External Input can be selected.) (DMI/CMI can be output simultaneously.)
Presets	TBT3, PCIe 4, PCIe 5, PCIe 6, PCIe 7

*: Connect a Coaxial Cable J1948A (0.4 m, SMA connector) and a Pick-off Tee J1793A (pick-off path) to the Noise Output, and define the measurement point at the end of the connection where a 34VKF50A and a Coaxial Cable J1821A (0.8 m, K connector) are connected to the OUT terminal of the J1793A.
⚠ Always use in combination with the Pick OFF Tee J1793A standard accessory.

External Input (for USB LFPS Signal Input)

Number of Channels	1
Number of Inputs Per Channel	2 (Differential)
Termination	50Ω, AC Coupling
Connector	SMA (J)
Input Amplitude	1.5 Vp-p Max. (Single-ended) 3.0 Vp-p Max. (Differential)
Output Control	ON and OFF can be selected. (Either DMI/CMI or External Input can be selected.)

Noise Generator MU195050A Specifications

Operating Bit Rate

Operating Bit Rate	2.4 Gbit/s to 32.1 Gbit/s

Data Input

Number of Channels	2
Number of Inputs per Channel	2 (Data, $\overline{\text{Data}}$) (Differential)
Input Amplitude	1.5 Vp-p max. (Single-end) 3.0 Vp-p max. (Differential)
Offset	–2.0 V to +3.3 V
Impedance	50Ω
Connector	K (J)

Data Output

The signal that is output from the noise source is AC-coupled.

Number of Channels	2
Number of Outputs per Channel	2 (Data, $\overline{\text{Data}}$) (Differential)
Insertion Loss	–3 dB +1/–2.5 dB*
Impedance	50Ω (Output Signal from noise source is AC-coupled)
Connector	K (J)

*: Defined for 12.890625 GHz and sinusoidal wave.

External Input

For connecting to USB3.1 Receiver Test Adapter G0373A or the Gating Output signal of MU195020A.

Number of Channels	1*
Number of Inputs Per Channel	2 (Differential)
Input Amplitude	1.5 Vp-p max. (Single-end) 3.0 Vp-p max. (Differential)
Impedance	50Ω, AC-coupled
Connector	SMA (f)

*: Data Input 1 Channel only

Differential Mode Interface (DMI)

The setting is common for Data Input 1 and Data Input 2. However, the Output Control can be turned On or Off individually.

Amplitude	4 mVp-p to 200 mVp-p (Differential)
Amplitude Setting Step	0.1 mV
Amplitude Accuracy	±20% ±10 mV*
Frequency	2 GHz to 10 GHz
Frequency Setting Step	10 MHz
Waveform	Sinusoidal wave
Presets	PCIe 3, PCIe 4, PCIe 5, PCIe 6
Output Control	Capability of switching On/Off of Data Input 1 Channel and Data Input 2 Channel simultaneously. (Either White Noise or External Input can be selected for Data Input 1 Channel). (Either Data Input 2 Channel or White Noise can be selected)

*: Defined at certain temperature between 20°C to 30°C for 2.1 GHz, 4.2 GHz, 10 GHz.

Common Mode Interface (CMI)

The setting is common for Data Input 1 and Data Input 2. However, the Output Control can be turned On or Off individually.

Amplitude	10 mVp-p to 250 mVp-p (Single-end)
Amplitude Setting Step	2 mV
Amplitude Accuracy	±20% ±25 mV*
Frequency	Low Band: 100 MHz to 1 GHz High Band: 1 GHz to 6 GHz
Frequency Setting Step	Low Band: 1 MHz High Band: 10 MHz
Waveform	Sinusoidal wave
Presets	TBT3, PCIe 4, PCIe 5, PCIe 6
Output Control	Capability of switching On/Off of Data Input 1 Channel and Data Input 2 Channel simultaneously. (Either DMI/CMI or External Input can be selected for Channel 1) (Either Channel 2 or DMI/CMI can be selected)

*: Defined at certain temperature between 20°C to 30°C for 120 MHz, 400 MHz, 1 GHz, 6 GHz.

Noise Generator MU195050A Specifications

White Noise

The setting is common for Data Input 1 and Data Input 2.

Flatness	±5 dB (10 MHz to 10 GHz)
Crest Factor	>5 (p-p/rms)
Amplitude	0.2 mV rms to 25 mV rms
Amplitude Setting Step	0.2 mV rms
Amplitude Accuracy	±20% ±2.5 mVrms*
On/Off	Capability of switching On/Off of Data Input 1 Channel and Data Input 2 Channel simultaneously. (Either DMI/CMI or External Input can be selected for Channel 1) (Either Channel 2 or DMI/CMI can be selected)

*: Defined at one specific temperature between 20°C to 30°C, subtracting the residual noise value from the data by sampling oscilloscope with 50 GHz bandwidth.

General

Dimensions and Mass	234 (W) × 21 (H) × 175 (D) mm (Excluding protrusions), 1.2 kg max.
Operating Temperature	+15°C to +35°C
Storage Temperature	–20°C to +60°C

32G baud NRZ/PAM4 Re-Driver MU196060A Specifications

Target Applications	PCIe 4.0: 16.0 Gbit/s, NRZ PCIe 5.0: 32.0 Gbit/s, NRZ PCIe 6.0: 32.0 Gbaud, PAM4 IEEE802.3bs 400GAUI-8 C2M: 26.5625 Gbaud, PAM4
Supported Plug-in Modules	MU196040B PAM4 ED MU195040A 21G/32G bit/s SI ED
Input Amplitude	**PAM4:** 0.40 to 0.80 Vp-p / Differential BER < 1E-8, 1E-12 (typ.), MCP, SSC 5300 ppm Down spread **NRZ:** 0.18 to 0.80 Vp-p / Differential BER < 1E-12, MCP, SSC 5300 ppm Down spread
Input/Output Connector	V (f)
LOSS Compensation	**PAM4:** 14 dB at 16.0 GHz, BER < 1E-6, 1E-9 (typ.), MCP, SSC 5300 ppm Down spread **NRZ:** 30 dB at 16.0 GHz, BER < 1E-12, MCP, SSC 5300 ppm Down spread
Clock Recovery (option)	With SSC support, PCIe 4.0, 5.0, 6.0

Synthesizer MU191000A Specifications

Clock Output

Number of Output	4
Frequency Range	100 MHz to 16.05 GHz (The clock accuracy and stability depend on the internal reference clock of the MP1900A or the external input reference clock; common setting with the AUX output.)
Frequency Setting Resolution	1 kHz
Offset from Set Frequency	–1000 ppm to +1000 ppm
Frequency Offset Setting Resolution	1 ppm
Level	0.7 Vp-p ±0.3 Vp-p (0.4 Vp-p to 1.0 Vp-p)
Duty	50% ±10%
Output Skew	≤10 ps (16.05 GHz)
Phase Noise	≤–110 dBc/Hz (10 kHz offset) ≤–111 dBc/Hz (100 kHz offset) ≤–110 dBc/Hz (1 MHz offset) (excluding non-harmonic spurious signals)
Internal SSC Modulation	SSC 33 kHz Center/Down Spread Selectable OFF/1500 ppm/3000 ppm/5000 ppm Selectable (PCIe 1 to 7 supported)
Termination	50Ω, AC Coupling
Connector	SMA (J)

10 MHz Reference Input

Frequency Range	10 MHz ±2 ppm
Level	0.5 Vp-p to 2.0 Vp-p
Termination	50Ω, AC Coupling
Connector	SMA (J)

10 MHz Reference Output

Level	1.0 Vp-p ±0.3 Vp-p (0.7 Vp-p to 1.3 Vp-p)
Waveform	Sinusoidal wave
Termination	50Ω, AC Coupling
Connector	SMA (J)

100 MHz Reference Input

Frequency Range	100 MHz/SSC 30 kHz to 33 kHz Center/Down Spread 0 to 5000 ppm
Amplitude	0.15 Vp-p to 1.45 Vp-p
Termination	50Ω, AC Coupling
Connector	SMA (J)

Reference Clock Source

Reference Clock Source	Internal/external 10 MHz or external 100 MHz can be selected.

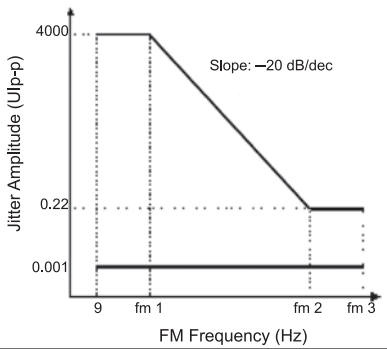
AUX Output

Number of Output	1
Level	0.5 Vp-p ±0.25 Vp-p (0.25 Vp-p to 0.75 Vp-p)
Duty	50% ±10%
Termination	50Ω, AC Coupling (Always apply a 50Ω termination to ensure proper operation.)
Connector	SMA (J)

12.5 GHz 4port Synthesizer MU181000B Specifications

Clock Output	Number of Output: 4 Frequency Range: 0.1 GHz to 12.5 GHz, Steps: 1 kHz/1 MHz Offset from Set Frequency: –1000 to +1000 ppm, Steps: 1 ppm, 1 Hz (Min) Level: 0.4 Vp-p to 1 Vp-p (AC) SSB Phase Noise: ≤–80 dBc/Hz (10 kHz offset) Intrinsic Jitter: ≤20 ps p-p, ≤20 ps p-p (fc>400 MHz) Waveform: Square wave (<1 GHz), Square wave or Sinusoidal wave (≥1 GHz) Duty: 50 ±10% Inter-channel Skew: ≤10 ps (12.5 GHz) Connector: SMA (f), Termination: 50Ω/GND
10 MHz Input	Frequency: 10 MHz ±10 ppm Level: 0.5 Vp-p to 2.0 Vp-p Waveform: Square wave or Sinusoidal wave Duty: 50 ±10% Connector: BNC, Termination: 50Ω/GND
10 MHz Output	Level: 1.0 Vp-p ±30% (AC) Waveform: Square wave Duty: 50 ±10% Connector: BNC, Termination: 50Ω/GND

Jitter Modulation Source MU181000B-001 Specifications

<table>
<tr><td>External Modulation Input</td><td>Frequency Range: 9 Hz to 1 GHz
Level Range: 3 Vp-p, 0 V(dc) (Max.)
Waveform: Sinusoidal wave
Connector: SMA (f), Termination: 50Ω/GND</td></tr>
<tr><td>External I, Q Input</td><td>Frequency Range: DC to 320 MHz (–3 dB)
Bandwidth Limit: 5 MHz (0.1 GHz ≤ fc ≤ 0.4 GHz), 10 MHz (0.4 GHz < fc ≤ 0.65 GHz), 20 MHz (0.65 GHz < fc ≤ 1.4 GHz),
100 MHz (1.4 GHz < fc ≤ 2.4 GHz), 320 MHz (2.4 GHz < fc ≤ 4.0 GHz)
Level Range: ±0.5 V
Connector: BNC, Termination: 50Ω/GND</td></tr>
<tr><td>100 MHz Reference Signal Input (SSC)</td><td>Output Center Frequency is × 25 or × 50 of Reference Input Frequency
Modulation Frequency: 30 kHz to 33 kHz
Frequency Deviation: 50 kHz
Level: 1.0 Vp-p ±30% (AC)
Waveform: Square wave or Sinusoidal wave
Duty: 50 ±10%
Connector: BNC, Termination: 50Ω/GND</td></tr>
<tr><td>Trigger Output</td><td>Available from 800 MHz to 12.5 GHz of Center frequency (fc)
Frequency: 1/64 (800 MHz < fc ≤ 6.4 GHz), 1/1 or 1/64 selectable (6.4 GHz < fc ≤ 12.5 GHz)
Level: 0.4 Vp-p to 1.1 Vp-p (AC)
Connector: SMA (f), Termination: 50Ω/GND</td></tr>
<tr><td>Internal Jitter Function</td><td>Modulation Frequency Range
<table>
<tr><th>Center Frequency (fc)</th><th>fm1</th><th>fm2</th><th>fm3</th></tr>
<tr><td>0.1 GHz to 0.8 GHz</td><td>13.75 Hz</td><td>250 kHz</td><td>5 MHz</td></tr>
<tr><td>0.8 GHz to 1.6 GHz</td><td>27.5 Hz</td><td>500 kHz</td><td>10 MHz</td></tr>
<tr><td>1.6 GHz to 3.2 GHz</td><td>55 Hz</td><td>1 MHz</td><td>20 MHz</td></tr>
<tr><td>3.2 GHz to 6.4 GHz</td><td>110 Hz</td><td>2 MHz</td><td>40 MHz</td></tr>
<tr><td>6.4 GHz to 12.5 GHz</td><td>220 Hz</td><td>4 MHz</td><td>80 MHz</td></tr>
</table>
Modulation Frequency Accuracy: ±100 ppm
Jitter Amplitude Accuracy:
±0.01 UI ±Q% (0.001 UIp-p to 2.19 UIp-p, fc <1 GHz)
±0.02 UI ±Q% (0.001 UIp-p to 2.19 UIp-p, fc ≥1 GHz)
±0.2 UI ±Q% (2.2 UIp-p to 21.99 UIp-p)
±2 UI ±Q% (22 UIp-p to 4000 UIp-p)
<table>
<tr><th>FM</th><th>Q</th></tr>
<tr><td>9 Hz ≤ fm ≤ 500 kHz</td><td>7</td></tr>
<tr><td>500 kHz < fm ≤ 2 MHz</td><td>12</td></tr>
<tr><td>2 MHz < fm ≤ 80 MHz</td><td>15</td></tr>
</table>
Jitter Mask
 
</td></tr>
<tr><td>External Jitter Function</td><td>Modulation Frequency Range: 9 Hz to 5 MHz (0.1 GHz ≤ fc ≤ 0.4 GHz)
9 Hz to 10 MHz (0.4 GHz < fc ≤ 0.65 GHz)
9 Hz to 20 MHz (0.65 GHz < fc ≤ 1.4 GHz)
9 Hz to 100 MHz (1.4 GHz < fc ≤ 2.4 GHz)
9 Hz to 500 MHz (2.4 GHz< fc ≤ 4.0 GHz)
9 Hz to 1 GHz (4.0 GHz< fc ≤ 12.5 GHz)
UI Range: 0.22, 2.0, 20, 200, 4000 UI
Modulation Frequency Range
<table>
<tr><th>Center Frequency</th><th>Input Frequency</th><th>Jitter Amplitude</th></tr>
<tr><td>1.4 GHz to 2.4 GHz</td><td>80 MHz to 100 MHz</td><td rowspan="4">Max. 0.22 UI</td></tr>
<tr><td>2.4 GHz to 4.0 GHz</td><td>80 MHz to 500 MHz</td></tr>
<tr><td>4.0 GHz to 8.0 GHz</td><td>80 MHz to 1 GHz</td></tr>
<tr><td rowspan="2">8.0 GHz to 8.5 GHz</td><td>80 MHz to 500 MHz</td></tr>
<tr><td>500 MHz to 1 GHz</td><td>Max. 0.10 UI</td></tr>
<tr><td>8.5 GHz to 11.3 GHz</td><td>80 MHz to 1 GHz</td><td>Max. 0.22 UI</td></tr>
<tr><td rowspan="2">11.3 GHz to 12.5 GHz</td><td>80 MHz to 250 MHz</td><td>Max. 0.22 UI</td></tr>
<tr><td>250 MHz to 1 GHz</td><td>Max. 0.10 UI</td></tr>
</table></td></tr>
</table>

Jitter Modulation Source MU181000B-001 Specifications

External Jitter Function

Modulation Sensitivity: 0.22 UI Range, Input level: 0.5 Vp-p

Output Clock Frequency	FM Frequency	Input Frequency	Jitter Amplitude
0.1 GHz ≤ fc ≤ 12.5 GHz	4 MHz	9 Hz to 4 MHz	0.1 UIp-p ±0.03 UI
	80 MHz	4 MHz to 80 MHz	
	500 MHz	80 MHz to 500 MHz	
2.4 GHz < fc ≤ 12.5 GHz	1 GHz	500 MHz to 1 GHz	

Modulation Sensitivity: 2, 20, 200, 4000 UI Range, Input level: 0.5 Vp-p

Clock Frequency: 0.1 GHz ≤ fc ≤ 0.8 GHz

Jitter Amplitude Category	FM Frequency	Input Frequency	Jitter Amplitude
2 UI	250 kHz	27.5 kHz	1 UIp-p ±0.3 UI
20 UI	27.5 kHz	2.75 kHz	10 UIp-p ±3 UI
200 UI	2.75 kHz	275 Hz	100 UIp-p ±30 UI
4000 UI	275 Hz	13.75 Hz	1000 UIp-p ±300 UI

Clock Frequency: 0.8 GHz < fc ≤ 1.6 GHz

Jitter Amplitude Category	FM Frequency	Input Frequency	Jitter Amplitude
2 UI	500 kHz	55 kHz	1 UIp-p ±0.3 UI
20 UI	55 kHz	5.5 kHz	10 UIp-p ±3 UI
200 UI	5.5 kHz	550 Hz	100 UIp-p ±30 UI
4000 UI	550 Hz	27.5 Hz	1000 UIp-p ±300 UI

Clock Frequency: 1.6 GHz < fc ≤ 3.2 GHz

Jitter Amplitude Category	FM Frequency	Input Frequency	Jitter Amplitude
2 UI	1 MHz	110 kHz	1 UIp-p ±0.3 UI
20 UI	110 kHz	11 kHz	10 UIp-p ±3 UI
200 UI	11 kHz	1.1 kHz	100 UIp-p ±30 UI
4000 UI	1.1 kHz	55 Hz	1000 UIp-p ±300 UI

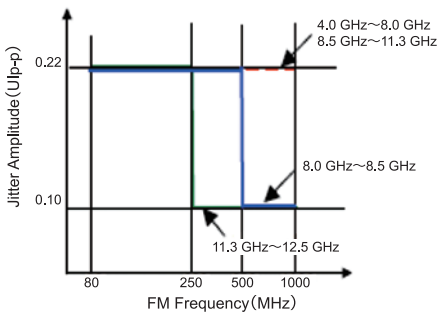
Clock Frequency: 3.2 GHz < fc ≤ 6.4 GHz

Jitter Amplitude Category	FM Frequency	Input Frequency	Jitter Amplitude
2 UI	2 MHz	220 kHz	1 UIp-p ±0.3 UI
20 UI	220 kHz	22 kHz	10 UIp-p ±3 UI
200 UI	22 kHz	2.2 kHz	100 UIp-p ±30 UI
4000 UI	2.2 kHz	110 Hz	1000 UIp-p ±300 UI

Clock Frequency: 6.4 GHz < fc ≤ 12.5 GHz

Jitter Amplitude Category	FM Frequency	Input Frequency	Jitter Amplitude
2 UI	4 MHz	440 kHz	1 UIp-p ±0.3 UI
20 UI	440 kHz	44 kHz	10 UIp-p ±3 UI
200 UI	44 kHz	4.4 kHz	100 UIp-p ±30 UI
4000 UI	4.4 kHz	220 Hz	1000 UIp-p ±300 UI

Jitter Mask



Triangle Wave Modulation

PCIe-I (2.5 GHz) or PCIe-II (5 GHz)
Clock Output Frequency Setting: Spread Method Center/Spread Method Down selectable
Frequency Offset: –1000 ppm to +1000 ppm, Steps: 1 ppm
Modulation Frequency Accuracy: 31.25 kHz ±1000 ppm
Frequency Deviation: ±6.25 MHz (PCIe-I, 2.5 GHz), ±12.5 MHz (PCIe-II, 5 GHz)
Deviation Accuracy: ±10%

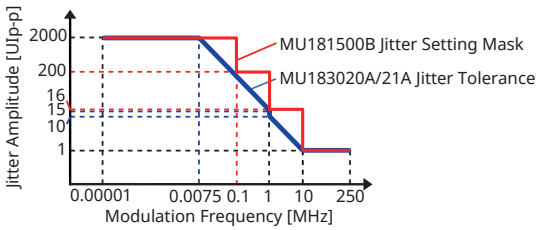
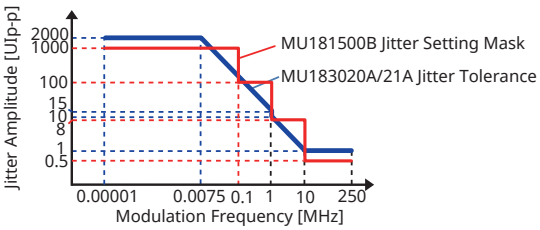
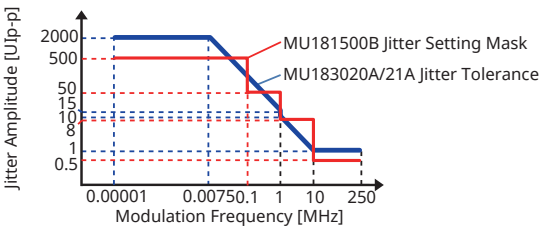
SSC Extension MU181000B-002 Specifications

100 MHz Reference Signal Input (SSC)

Outputs either 100 MHz with phase deviation x25, x50, or x80 frequency-multiplied clock from Clock Output connector
Supports PCI Express Host Reflclk input
Modulation Frequency: 30 kHz to 33 kHz
Frequency Deviation: 500 kHzp-p max.
Level: 0.15 Vp-p to 1.3 Vp-p (AC)
Waveform: Square wave or Sinusoidal wave
Duty: 50 ±10%
Connector: BNC

Jitter Modulation Source MU181500B Specifications

External Clock Input	Number of Input: 1 Frequency Range: 6.400 001 GHz to 12.500 000 GHz (MU181000B, Combination: On) 0.800 000 GHz to 15.000 000 GHz (MU181000B, Combination: Off, or External synthesizer) Amplitude: 0.4 Vp-p to 1.0 Vp-p Connector: SMA (f), Termination: 50Ω/AC Coupling
External Jitter Input	Number of Input: 1 Frequency Range: 10 kHz to 1 GHz Amplitude: 0 to 2.0 Vp-p Connector: SMA (f), Termination: 50Ω/GND
Jittered Clock Output	Number of Output: 2 Frequency Range: 0.800 001 GHz to 1.562 500 GHz (MU181000B, Combination: On), Steps: 0.000 001 GHz 1.600 001 GHz to 3.125 000 GHz (MU181000B, Combination: On), Steps: 0.000 001 GHz 3.200 001 GHz to 6.250 000 GHz (MU181000B, Combination: On), Steps: 0.000 001 GHz 6.400 001 GHz to 12.500 000 GHz (MU181000B, Combination: On), Steps: 0.000 001 GHz 12.800 002 GHz to 15.000 000 GHz (MU181000B, Combination: On), Steps: 0.000 002 GHz 0.8 GHz to 15 GHz (MU181000B, Combination: Off, or External synthesizer) Frequency Offset: 1000 to +1000 ppm (MU181000B, Combination: On), Steps: 1 ppm None (MU181000B, Combination: Off, or External synthesizer) Amplitude: 0.4 Vp-p (Min.), 1.0 Vp-p (Max.) Intrinsic Jitter: ≤350 fs (4.25, 7.0125, 10, 12.5, 14, 15 GHz) Connector: SMA (f), Termination: 50Ω/AC Coupling
IQ Output	Number of Output: 2 (I, Q) Amplitude: 1 Vp-p (Max.) Connector: SMA (f), Termination: 50Ω/GND
AUX Input	Number of Input: 1 Frequency Range: Same frequency with External Clock Input Amplitude: 0.4 Vp-p (Min.), 1.1 Vp-p (Max.) Connector: SMA (f), Termination: 50Ω/AC Coupling
Reference Clock Output	Number of Output: 2 Reference Clock: External Clock Input or AUX Input (MU181000B, Combination: On) External Clock Input (MU181000B, Combination: Off, or External synthesizer) Frequency Range: 1/N of Jittered Clock Output Frequency (N: 1, 2, or 4) Amplitude: 0.4 Vp-p (Min.), 1.0 Vp-p (Max.) (Jittered Clock Output Frequency: ≥4 GHz) 0.4 Vp-p (Min.), 1.2 Vp-p (Max.) (Jittered Clock Output Frequency: <4 GHz) Connector: SMA (f), Termination: 50Ω/AC Coupling
Sub-rate Clock Output	Number of Output: 2 (Differential) Frequency Range: 1/N of Jittered Clock Output Frequency (N: 8 to 256, Steps: 1) Amplitude: 0.1 Vp-p to 0.7 Vp-p, Steps: 10 mV Accuracy: ±70 mV ±20% of Amplitude (N: 8) Connector: SMA (f), Termination: 50Ω/AC Coupling

Internal Sinusoidal Jitter (SJ1)	32G PPG Full rate Clock Out setting, Bit-rate: 15 Gbit/s to 32.1 Gbit/s Half rate Clock Out setting, Bit-rate: 2.4 Gbit/s to 32.1 Gbit/s  Full rate Clock Out setting, Bit-rate: 4 Gbit/s to 15 Gbit/s  Full rate Clock Out setting, Bit-rate: 2.4 Gbit/s to 4 Gbit/s  32G PPG (Full rate Clock Out, Bit-rate: 4 Gbit/s to 15 Gbit/s) 0 to 1000 UIp-p (FM: 10 Hz to 100 kHz), Steps: 0.001 UI 0 to 100 UIp-p (FM: 100.1 kHz to 1 MHz), Steps: 0.001 UI 0 to 8 UIp-p (FM: 1.001 MHz to 10 MHz), Steps: 0.001 UI 0 to 0.5 UIp-p (FM: 10.01 MHz to 100 MHz), Steps: 0.001 UI 32G PPG (Full rate Clock Out, Bit-rate: 2.4 Gbit/s to 4 Gbit/s) 0 to 500 UIp-p (FM: 10 Hz to 100 kHz), Steps: 0.001 UI 0 to 50 UIp-p (FM: 100.1 kHz to 1 MHz), Steps: 0.001 UI 0 to 8 UIp-p (FM: 1.001 MHz to 10 MHz), Steps: 0.001 UI 0 to 0.5 UIp-p (FM: 10.01 MHz to 250 MHz), Steps: 0.001 UI 32G PPG (Full rate Clock Out, Bit-rate: 15 Gbit/s to 30 Gbit/s, Half rate Clock Out, Bit-rate: 2.4 Gbit/s to 30 Gbit/s) 0 to 2000 UIp-p (FM: 10 Hz to 100 kHz), Steps: 0.002 UI 0 to 50 UIp-p (FM: 100.1 kHz to 1 MHz), Steps: 0.002 UI 0 to 8 UIp-p (FM: 1.001 MHz to 10 MHz), Steps: 0.002 UI 0 to 0.5 UIp-p (FM: 10.01 MHz to 250 MHz), Steps: 0.002 UI 32G PPG (Full rate Clock Out, Half rate Clock Out, Bit-rate: 30 Gbit/s to 32.1 Gbit/s) 0 to 2000 UIp-p (FM: 10 Hz to 100 kHz), Steps: 0.004 UI 0 to 200 UIp-p (FM: 100.1 kHz to 1 MHz), Steps: 0.004 UI 0 to 16 UIp-p (FM: 1.001 MHz to 10 MHz), Steps: 0.004 UI 0 to 1 UIp-p (FM: 10.01 MHz to 150 MHz), Steps: 0.004 UI Accuracy: ±0.03 UI ±Q% (Amplitude: 0.001 UIp-p to 2.199 UIp-p) ±0.2 UI ±Q% (Amplitude: 2.2 UIp-p to 21.999 UIp-p) ±2 UI ±Q% (Amplitude: 22 UIp-p to 219.999 UIp-p) ±20 UI ±Q% (Amplitude: 220 UIp-p to 2000 UIp-p) FW / Q 10Hz to 500 kHz / 7 500.1 kHz to 2 MHz / 10 2.01 MHz to 80 MHz / 13 80.01 MHz to 250 MHz / 15 On/Off Function: supported

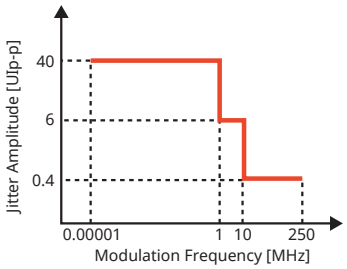
Jitter Modulation Source MU181500B Specifications

External Sinusoidal Jitter (SJ2)
[MU181000B-001]

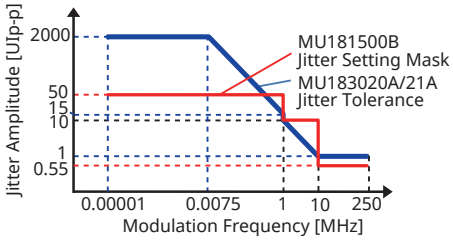
Jitter Setting Mask

Jittered Clock Output Frequency: 6.400 001 GHz to 15 GHz

Full Rate Mode
Bit-rate: 6.400 001 Gbit/s to 15 Gbit/s

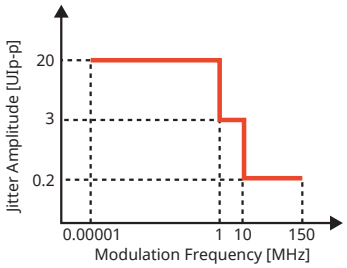


Half Rate Mode
Bit-rate: 12.800 001 Gbit/s to 30 Gbit/s
Quarter Rate Mode
Bit-rate: 25.600 004 Gbit/s to 32.1 Gbit/s

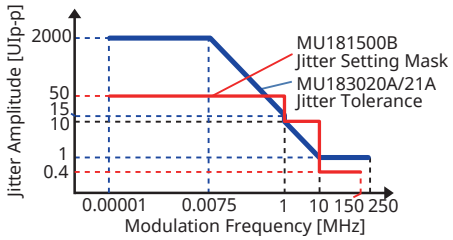


Jittered Clock Output Frequency: 3.200 001 GHz to 6.25 GHz

Full Rate Mode
Bit-rate: 3.200 001 Gbit/s to 6.25 Gbit/s

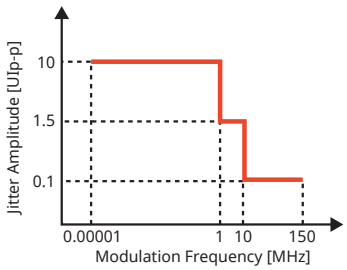


Half Rate Mode
Bit-rate: 8 Gbit/s to 12.5 Gbit/s

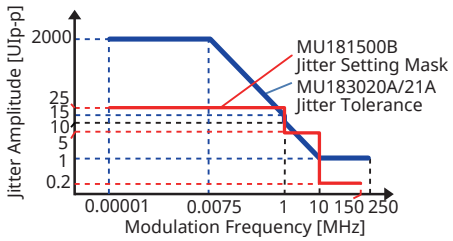


Jittered Clock Output Frequency: 1.800 001 GHz to 3.125 GHz

Full Rate Mode
Bit-rate: 1.800 001 Gbit/s to 3.125 Gbit/s

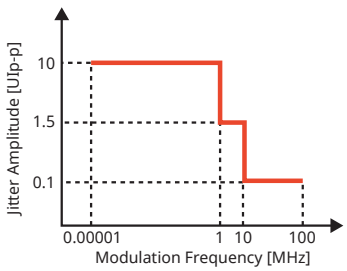


Half Rate Mode
Bit-rate: 3.600 002 Gbit/s to 6.25 Gbit/s

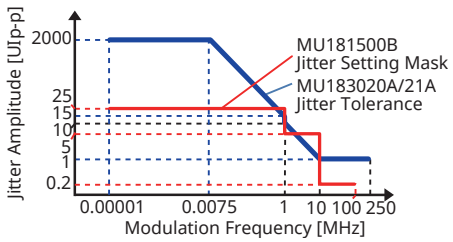


Jittered Clock Output Frequency: 1.600 001 GHz to 1.8 GHz

Full Rate Mode
Bit-rate: 1.600 001 Gbit/s to 1.8 Gbit/s

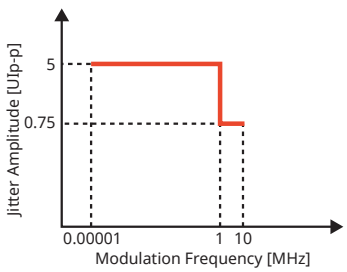


Half Rate Mode
Bit-rate: 3.200 002 Gbit/s to 3.6 Gbit/s

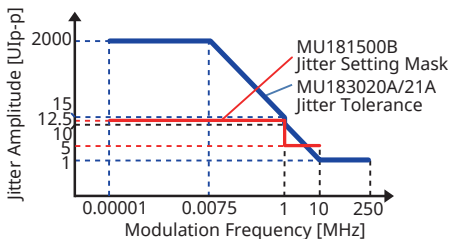


Jittered Clock Output Frequency: 0.800 001 GHz to 1.562 5 GHz

Full Rate Mode
Bit-rate: 0.800 001 Gbit/s to 1.562 5 Gbit/s



Half Rate Mode
Bit-rate: 1.600 002 Gbit/s to 3.125 Gbit/s



External Sinusoidal Jitter (SJ2) [MU181000B-001]

Modulation Frequency (FM): 10 Hz to 10 kHz, Steps: 1 Hz
10 kHz to 100 kHz, Steps: 10 Hz
100 kHz to 1 MHz, Steps: 100 Hz
1 MHz to 10 MHz, Steps: 1 kHz
10 MHz to 100 MHz, Steps: 10 kHz
100 MHz to 250 MHz, Steps: 100 kHz

Accuracy: ±100 ppm

Amplitude:

Full Rate Mode

Bit-rate: 6.400 001 Gbit/s to 15 Gbit/s
- 0 to 40 UIp-p (FM: 10 Hz to 1 MHz), Steps: 0.001 UI
- 0 to 6 UIp-p (FM: 1.001 MHz to 10 MHz), Steps: 0.001 UI
- 0 to 0.4 UIp-p (FM: 10.01 MHz to 250 MHz), Steps: 0.001 UI

Bit-rate: 3.200 001 Gbit/s to 6.25 Gbit/s
- 0 to 20 UIp-p (FM: 10 Hz to 1 MHz), Steps: 0.001 UI
- 0 to 3 UIp-p (FM: 1.001 MHz to 10 MHz), Steps: 0.001 UI
- 0 to 0.2 UIp-p (FM: 10.01 MHz to 150 MHz), Steps: 0.001 UI

Bit-rate: 1.800 001 Gbit/s to 3.125 Gbit/s
- 0 to 10 UIp-p (FM: 10 Hz to 1 MHz), Steps: 0.001 UI
- 0 to 1.5 UIp-p (FM: 1.001 MHz to 10 MHz), Steps: 0.001 UI
- 0 to 0.1 UIp-p (FM: 10.01 MHz to 150 MHz), Steps: 0.001 UI

Bit-rate: 1.600 001 Gbit/s to 1.8 Gbit/s
- 0 to 10 UIp-p (FM: 10 Hz to 1 MHz), Steps: 0.001 UI
- 0 to 1.5 UIp-p (FM: 1.001 MHz to 10 MHz), Steps: 0.001 UI
- 0 to 0.1 UIp-p (FM: 10.01 MHz to 100 MHz), Steps: 0.001 UI

Bit-rate: 0.800 001 Gbit/s to 1.562 5 Gbit/s
- 0 to 5 UIp-p (FM: 10 Hz to 1 MHz), Steps: 0.001 UI
- 0 to 0.75 UIp-p (FM: 1.001 MHz to 10 MHz), Steps: 0.001 UI

Half Rate Mode

Bit-rate: 12.800 001 Gbit/s to 30 Gbit/s
- 0 to 50 UIp-p (FM: 10 Hz to 1 MHz), Steps: 0.2 UI
- 0 to 10 UIp-p (FM: 1.001 MHz to 10 MHz), Steps: 0.02 UI
- 0 to 0.55 UIp-p (FM: 10.01 MHz to 250 MHz), Steps: 0.002 UI

Bit-rate: 8 Gbit/s to 12.5 Gbit/s
- 0 to 50 UIp-p (FM: 10 Hz to 1 MHz), Steps: 0.2 UI
- 0 to 10 UIp-p (FM: 1.001 MHz to 10 MHz), Steps: 0.02 UI
- 0 to 0.4 UIp-p (FM: 10.01 MHz to 150 MHz), Steps: 0.002 UI

Bit-rate: 3.600 002 Gbit/s to 6.25 Gbit/s
- 0 to 25 UIp-p (FM: 10 Hz to 1 MHz), Steps: 0.2 UI
- 0 to 5 UIp-p (FM: 1.001 MHz to 10 MHz), Steps: 0.02 UI
- 0 to 0.2 UIp-p (FM: 10.01 MHz to 150 MHz), Steps: 0.002 UI

Bit-rate: 3.200 002 Gbit/s to 3.6 Gbit/s
- 0 to 25 UIp-p (FM: 10 Hz to 1 MHz), Steps: 0.2 UI
- 0 to 5 UIp-p (FM: 1.001 MHz to 10 MHz), Steps: 0.02 UI
- 0 to 0.2 UIp-p (FM: 10.01 MHz to 100 MHz), Steps: 0.002 UI

Bit-rate: 1.600 002 Gbit/s to 3.125 Gbit/s
- 0 to 12.5 UIp-p (FM: 10 Hz to 1 MHz), Steps: 0.2 UI
- 0 to 2.5 UIp-p (FM: 1.001 MHz to 10 MHz), Steps: 0.02 UI

Quarter Rate Mode

Bit-rate: 25.600 004 Gbit/s to 32.1 Gbit/s
- 0 to 50 UIp-p (FM: 10 Hz to 1 MHz), Steps: 0.004 UI
- 0 to 10 UIp-p (FM: 1.001 MHz to 10 MHz), Steps: 0.004 UI
- 0 to 0.548 UIp-p (FM: 10.01 MHz to 250 MHz), Steps: 0.004 UI

Accuracy: ±0.03 UI ±Q% (Amplitude: 0.002 UIp-p to 2.19 UIp-p)
±0.2 UI ±Q% (Amplitude: 2.2 UIp-p to 21.9 UIp-p)
±2 UI ±Q% (Amplitude: 22 UIp-p to 50 UIp-p)

FW	Q
10 Hz ≤ fm ≤ 500 kHz	10
500 kHz < fm ≤ 2 MHz	13
2 MHz < fm≤80 MHz	15
80 MHz < fm ≤ 250 MHz	18

On/Off Function: Supported

Spread Spectrum Clocking (SSC)

SSC Profile: Triangular, USB4, Variable
Type: Down-Spread, Center-Spread, Up-Spread, Asymmetric
Modulation Frequency: 28 kHz to 37 kHz, Steps: 1 Hz
Accuracy: ±100 ppm
Deviation: 0 to 7000 ppm, Steps: 1 ppm
Modulation
- Periodic Burst: Repeatedly outputs Asymmetric SSC
- Continuous: Outputs Triangular waveform after single Asymmetric SSC output

On/Off Function: Supported

Jitter Modulation Source MU181500B Specifications

Random Jitter (RJ)

Bandwidth: 10 kHz to 1 GHz
Crest Factor: 16 dB
Filter Type
User Filter
Filter: 10 MHz, 20 MHz, Through (HPF 3 dB bandwidth)
100 MHz, Through (LPF 3 dB bandwidth)
Amplitude
Full Rate Mode

Jittered Clock Output Frequency [GHz]	Setting Range [UIp-p]	Steps [mUI]
≥2.5	0 to 0.5	2
<2.5	0 to 0.2f	2

Half Rate Mode*1

Jittered Clock Output Frequency [GHz]	Setting Range [UIp-p]	Steps [mUI]
≥2.5	0 to 0.5	4
<2.5	0 to 0.2f	4

Quarter Rate Mode

Jittered Clock Output Frequency [GHz]	Setting Range [UIp-p]	Steps [mUI]
≥2.5	0 to 0.496	8
<2.5	0 to 2f	8

f: Jittered Clock Output Frequency [GHz]

Accuracy: ±4.9 ps ±15% (Jittered Clock Output Frequency: ≥4 GHz)
±7.0 ps ±15% (Jittered Clock Output Frequency: <4 GHz)

PCIe (Data clocked) or PCIe (Common Ref. clock) Filter
Filter: LF (10 kHz to 1.5 MHz) or HF (1.5 MHz to 100 MHz) for PCIe
Amplitude
Full Rate Mode

Jittered Clock Output Frequency [GHz]	LF and HF Setting Range [ps rms]	Steps [ps rms]
≥4	0 to 8.8	0.1

Half Rate Mode

Jittered Clock Output Frequency [GHz]	LF and HF Setting Range [ps rms]	Steps [ps rms]
≥4	0 to 8.8	0.2

Quarter Rate Mode

Jittered Clock Output Frequency [GHz]	LF and HF Setting Range [ps rms]	Steps [ps rms]
≥4	0 to 8.8	0.4

LF Amplitude ≥ HF Amplitude
Accuracy: ±0.6 ps ±10%

On/Off Function: Supported

Bounded Uncorrelated Jitter (BUJ)

PRBS Pattern Length: $2^n - 1$ (n = 7, 9, 11, 15, 23, or 31)
BUJ Rate: 0.1 Gbit/s to 3.2 Gbit/s, Steps: 1 k bit/s
4.9 Gbit/s to 6.25 Gbit/s, Steps: 1 k bit/s (Jittered Clock Output Frequency: >4 GHz)
9.8 Gbit/s to 12.5 Gbit/s, Steps: 1 k bit/s (Jittered Clock Output Frequency: >4 GHz)
Filter Type (LPF 3 dB Bandwidth): 50, 100, 200, 300, 500 MHz, Through (Jittered Clock Output Frequency: >4 GHz)
50, 100, 200, 300 MHz, Through (Jittered Clock Output Frequency: ≤4 GHz)
Amplitude:
Full Rate Mode

Jittered Clock Output Frequency [GHz]	Setting Range [UIp-p]	Steps [mUI]
≥2.5	0 to 0.5	2
<2.5	0 to 0.2f	2

Half Rate Mode

Jittered Clock Output Frequency [GHz]	Setting Range [UIp-p]	Steps [mUI]
≥2.5	0 to 0.5	4
<2.5	0 to 0.2f	4

f: Jittered Clock Output Frequency [GHz]

Accuracy: ±4.9 ps ±15% (Jittered Clock Output Frequency: ≥4 GHz)
±7.0 ps ±15% (Jittered Clock Output Frequency: <4 GHz)
PRBS Pattern Length: $2^n - 1$ (n = 7, 9)
BUJ Rate: 6, 5.5, 4.9 Gbit/s, LPF 500 MHz
BUJ Rate: 3.2 Gbit/s, 3 Gbit/s, LPF 300 MHz
BUJ Rate: 3.2 Gbit/s, 2 Gbit/s, LPF 200 MHz
BUJ Rate: 2 Gbit/s, 1.1 Gbit/s, LPF 100 MHz
On/Off Function: Supported

External Jitter

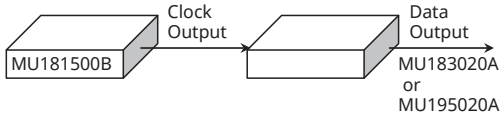
Bandwidth: 10 kHz to 1 GHz
Accuracy*1: 0.5 UI ±10% (2 Vp-p)
Linearity*1: ±6 ps ±10%
On/Off Function: Supported

*1: Jittered Clock Output Frequency: Specified as 5 GHz, Modulation Frequency: 0.5 GHz, Sinusoidal Jitter

Jitter Modulation Source MU181500B Specifications

<table>
<tr><td>SJ2 Switching</td><td>Function for switching built-in SJ2 and MU181000B-001 input</td></tr>
<tr><td>Built-in SJ2*2, *3, *4</td><td>
Modulation Frequency: 33 kHz, 100 MHz, 210 MHz
Bandwidth:
<table>
<tr><th>Clock Frequency</th><th>Bandwidth</th></tr>
<tr><td>0.8 GHz < Fc ≤ 1.2 GHz</td><td>33 kHz</td></tr>
<tr><td>1.2 GHz < Fc ≤ 8.5 GHz</td><td>33 kHz, 100 MHz</td></tr>
<tr><td>4 GHz < Fc ≤ 8.5 GHz*3</td><td>33 kHz, 100 MHz, 210 MHz</td></tr>
<tr><td>8.5 GHz < Fc ≤ 15 GHz</td><td>33 kHz, 100 MHz, 210 MHz</td></tr>
</table>
Accuracy: ±100 ppm
Amplitude Setting Range:
<table>
<tr><th rowspan="3">Modulation Frequency</th><th colspan="4">Data Pattern Generator</th></tr>
<tr><th colspan="2">Full-rate (PPG), Full-rate (MUX)</th><th colspan="2">Half-rate (MUX)</th></tr>
<tr><th>Setting Range [UIp-p]</th><th>Step [UI]</th><th>Setting Range [UIp-p]</th><th>Step [UI]</th></tr>
<tr><td>33 kHz</td><td>0 to 40</td><td>0.001</td><td>0 to 50</td><td>0.002</td></tr>
<tr><td>100 MHz</td><td>0 to 0.25</td><td>0.001</td><td>0 to 0.5</td><td>0.002</td></tr>
<tr><td>210 MHz</td><td>0 to 0.125</td><td>0.001</td><td>0 to 0.25</td><td>0.002</td></tr>
</table>
<table>
<tr><th rowspan="3">Modulation Frequency</th><th colspan="2">Data Pattern Generator</th></tr>
<tr><th colspan="2">Quarter-rate (MUX)</th></tr>
<tr><th>Setting Range [UIp-p]</th><th>Step [UI]</th></tr>
<tr><td>33 kHz</td><td>0 to 50</td><td>0.004</td></tr>
<tr><td>100 MHz</td><td>0 to 0.5</td><td>0.004</td></tr>
<tr><td>210 MHz</td><td>0 to 0.248</td><td>0.004</td></tr>
</table>
<table>
<tr><th rowspan="3">Modulation Frequency</th><th colspan="4">Data Pattern Generator</th></tr>
<tr><th colspan="2">32G PPG*5</th><th colspan="2">32G PPG*6</th></tr>
<tr><th>Setting Range [UIp-p]</th><th>Step [UI]</th><th>Setting Range [UIp-p]</th><th>Step [UI]</th></tr>
<tr><td>33 kHz</td><td>0 to 500</td><td>0.001</td><td>0 to 500</td><td>0.001</td></tr>
<tr><td>100 MHz</td><td>0 to 0.25</td><td>0.001</td><td>0 to 8</td><td>0.001</td></tr>
<tr><td>210 MHz</td><td>0 to 0.125</td><td>0.001</td><td>—</td><td>—</td></tr>
</table>
<table>
<tr><th rowspan="3">Modulation Frequency</th><th colspan="4">Data Pattern Generator</th></tr>
<tr><th colspan="2">32G PPG*7</th><th colspan="2">32G PPG*8</th></tr>
<tr><th>Setting Range [UIp-p]</th><th>Step [UI]</th><th>Setting Range [UIp-p]</th><th>Step [UI]</th></tr>
<tr><td>33 kHz</td><td>0 to 1000</td><td>0.002</td><td>0 to 1000</td><td>0.004</td></tr>
<tr><td>100 MHz</td><td>0 to 0.5</td><td>0.002</td><td>0 to 0.5</td><td>0.004</td></tr>
<tr><td>210 MHz</td><td>0 to 0.25</td><td>0.002</td><td>0 to 0.248</td><td>0.004</td></tr>
</table>
Accuracy: ±0.03 UI ±Q% (Amplitude: 0.001 UIp-p to 2.199 UIp-p)
±0.2 UI ±Q% (Amplitude: 2.2 UIp-p to 21.999 UIp-p)
±2 UI ±Q% (Amplitude: 22 UIp-p to 219.999 UIp-p)
±20 UI ±Q% (Amplitude: 222 UIp-p to 2000 UIp-p)
<table>
<tr><th>FW</th><th>Q</th></tr>
<tr><td>33 kHz</td><td>7</td></tr>
<tr><td>100 MHz, 210 MHz*9</td><td>15</td></tr>
</table>
Output Setting; On/Off switching
</td></tr>
</table>

*2: The Built-in SJ2 function is used by the MX190000A V2.00.00 and later. Either the Built-in SJ2 or SJ2 via MU181000 function can be selected, but both functions cannot be used simultaneously.
*3: When Data Pattern Generator is 32G PPG or SI PPG, or in other words when main unit and 32G PPG or SI PG are linked.
*4: Specifications for MU183020A or MU195020A Data output on following figure



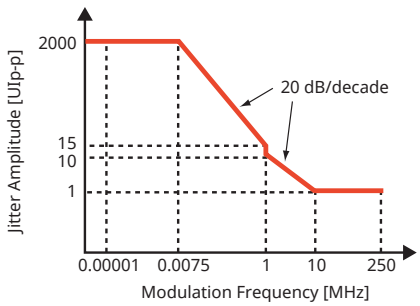
*5: At Data rate of 4 Gbit/s to 15 Gbit/s when Full-rate Clock Out set
*6: At Data rate of 2.4 Gbit/s to 4 Gbit/s when Full-rate Clock Out set
*7: At Data rate of 15 Gbit/s to 30 Gbit/s when Full-rate Clock Out, or at Data rate of 2.4 Gbit/s to 30 Gbit/s when Half-rate Clock Out set
*8: At Data rate of 30 Gbit/s to 32.1 Gbit/s when Full-rate Clock Out or Half-rate Clock Out set
*9: Typical value at 4 GHz ≤ FC ≤ 8.5 GHz

High-Speed Serial Data Test Software MX183000A Specifications

Operation Conditions

Install Destination	MP1900A or PC
PC Specifications	OS: English or Japanese Windows 7 Professional/Enterprise/Ultimate CPU: 1 GHz min. Memory: 1 GB min. (for Windows 7, 32-bit) 2 GB min. (for Windows 7, 64-bit) Hard Disk: Free space 2 GB min. Remote Interface: Ethernet (10BASE-T, 100BASE-TX) Display: Resolution 800 × 600 min., 32-bit color
Control Target	MP1900A Controlled Units: 3 units max. Version: MX190000A Installer: Version 1.00.00 or later

Jitter Tolerance Test (MX183000A-PL001)

Run Test/Stop Test	Starts and stop Jitter Tolerance Test
Jitter Tolerance Table	JTOL Measurement Point Setting Sets measured SJ modulation frequency and Pass/Fail modulation degree (UI), and set search modulation range Jitter Frequency Setting Range Sets each of Jitter Freq. [Hz], Mask [UI], Upper Limit [UI], Lower Limit [UI], Upper Ratio, Lower Ratio Setting range depends on Jitter modulation source MU181500B Jitter Amplitude Setting Range  Note that available jitter frequency and jitter amplitude for jitter measurement depend on the clock frequency set by controller and MU181500B. Set All Limit Resets the Upper Limit and Lower Limit values at the ratio set for Mask. Set the ratio to reset for Upper Ratio and Lower Ratio. Upper Ratio: 1.000 to 1000, 0.001 steps Lower Ratio: 0.001 to 1.000, 0.001 steps Measurement Sequence: From higher Freq. side, From lower Freq. side
JTOL Setting	Detection Unit: Error Rate, Error Count, Estimate, Symbol Error Rate, Bit Error Rate, MSB Error Rate, LSB Error Rate Error Threshold: 1E–3 to 1E-12, E–1 steps Error Count: 0 to 10000000, 1 steps BER for JTOL Estimation: 1.0E–20 to 9.9E–9
Auto Search	OFF/FINE/COARSE
Search	Direction Search: Binary, Downwards Linear, Downwards Log, Upwards Linear, Upwards Log, Binary + Linear Step: When Downwards/Upwards Linear is selected Jitter Freq. ≤ 100 kHz 0.001 to 2000.000 0.001 step 100k < Jitter Freq. ≤ 1 MHz 0.001 to 200.000 0.001 step 1M < Jitter Freq. ≤ 10 MHz 0.001 to 15.000 0.001 step 10 MHz < Jitter Freq. 0.001 to 1.000 0.001 step Ratio: When Downwards/Upwards Log is selected Jitter Freq. ≤ 100 kHz, 100k < Jitter Freq. ≤ 1 MHz, 1M < Jitter Freq. ≤ 10 MHz, 10 MHz < Jitter Freq. 0.01 to 1.00 0.001 step
Timer [sec.]	Waiting, Setting: 1 to 99 seconds, in steps of one second Gating: 1 to 86400 seconds, in steps of one second
Graph Tab	Display: OFF/ON BER for JTOL Estimation: 1.0E–20 to 9.9E–9, 0.1 step, E–1 step
Report Tab	Make HTML/CSV: Displays the Jitter Tolerance results in HTML or CSV.

High-Speed Serial Data Test Software MX183000A Specifications

PCIe Link Training (MX183000A-PL021, MX183000A-PL025*, MX183000A-PL026*)

Specification	1.0/1.1 (2.5 GT/s), 2.0 (5 GT/s), 3.0/3.1 (8 GT/s), 4.0 (16 GT/s). 5.0 (32 GT/s)*, 6.0 (64 GT/s)*
Link Start/Stop/Unlink	Starts PCIe Link Training (PCIe 1.0 to 6.0*) Continues sending Test Pattern after Link Training
BER Measurement	Clicking button after Link Training measures BER. Selecting PCIe 1.0, 2.0, or 3.0 in Specification disables function when using MU196040B PAM4 ED and MU196060A Re-Driver.
BER Monitor	ON/OFF
Matrix Scan	Measures BER at cursor and maps results Selecting PCIe 1.0, 2.0, or 3.0 in Specification disables function when using MU196040B PAM4 ED and MU196060A Re-Driver.
FS (Full Swing)	24, 48, 63
LF (Low Frequency)	Sets 8, 16, or 21 automatically according to FS setting
LTSSM Log	Displays LTSSM transition log during Link Training
Export CSV	Saves Log as csv file
Loopback Method	PCIe 1.0 to 4.0: Configuration, Recovery PCIe 5.0*: Config EQ Bypass to 32G, Config No EQ, Recovery EQ Bypass to 32G, Recovery Full EQ PCIe 6.0*: Config EQ Bypass to 64G, Config No EQ, Recovery EQ Bypass to 64G, Recovery Full EQ
Test Pattern	
Compliance	MCP/CP
PRBS	PRBS7, PRBS9, PRBS10, PRBS11, PRBS15, PRBS20, PRBS23, PRBS31
Flit	Selectable only with PCIe 6.0
USER	
Clock Architecture	Common, SRIS, SRNS
SSC	5000 ppm, 3000 ppm, OFF
SKP	
Insertion	ON/OFF
Filtering	ON/OFF
Timeout	Sets timeout at each LTSSM State
LTSSM Trigger	Outputs trigger from PPG Aux Output at transition to specified LTSSM State

*: The PL025 option expands PL021 support to PCIe 5.0. PL025 requires the PL021 option.
The PL026 option expands PL025 support to PCIe 6.0. PL026 requires both the PL025 and the PL021 option.

USB Link Training (MX183000A-PL022, MX183000A-PL023*[1])

Link Start/Stop/Unlink	Starts USB Link Training(USB3.1 Gen1/Gen2) when LFPS is detected by Data Input of MU195040A. Continues sending test patterns after Link Training.
Specification	Gen1×1 (5.0 GT/s ×1), Gen1×2 (5.0 GT/s ×2), Gen2×1 (10.0 GT/s ×1), Gen2×2 (10.0 GT/s ×2)
Not Wait for The LFPS Signal	Supports simultaneous 2-Lane BER measurement when GenX×2 selected
BER Measurement	Click the button after Link Training is sent to execute the BER measurement. Supports simultaneous 2-Lane BER measurement when GenX×2 selected
BER Monitor	ON/OFF
LTSSM Log	Displays transition logs of LTSSM.
LTSSM Log Items	Time, ΔTime, State (Lane0), State (Lane1), Speed[GT/s], HEX Dump (Lane0), HEX Dump (Lane1)
Export CSV	Saves logs in csv format.
Send Ping LFPS	Outputs Ping LFPS signal. Switches DUT CP when performing Tx test of USB Compliance Test.
Test Pattern	Compliance/USER
Timeout	Sets Timeout for each LTSSM State.
Result Display of USB Link Training	
Common Parameter	LTSSM State, Linkup Speed
8b10b Counters	SKP Count*[2], Symbol Err, Current RD Err, Symbol Lock
128b132b Counters	SKP Count*[2], TS1/TS2 Symbol14-15 DC Balance*[2], Sync Header Err, TS1 OS Parity Err, Block Lock, SYNCOS Counter*[2]

*1: Supports USB Link Training (USB3.1 Gen1/2) (only enabled for PL022). Support for USB Link Training (USB3.2 Gen1/2 ×1/×2) (enabled for PL022 and PL023).
*2: Displays both Transmitted and Received.

DUT Error Counts Import (MX183000A-PL031)

DUT Control Tab	Allows you to select and run external programs for controlling DUT.
Initialize	Allows you to select a program for initializing DUT.
Measurement	Allows you to select a program for measuring DUT.
Finalize	Allows you to select a program for finalizing DUT.
Log Viewer button	Displays the log window.
Finalize button	Runs the selected Finalize program.
Initialize button	Runs the selected Initialize program.
BER Measure Tab	Allows starting and stopping BER measurement, and displaying the measurement results.
Result	Displays the measurement results, which are: error rates, error counts, and whether alarms are given or not.
Cycle	Changes measurement cycle (Single/Repeat).
Start/Stop	Starts or stops the measurement.
Abort	Aborts the measurement.
Debug	Executes the measure programs, ignoring syntax errors.

Anritsu Advancing beyond

Specifications are subject to change without notice.

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Printed in Japan 28/MAY/2026 ddcm/CDT Catalog No. MP1900A_Datasheet-E-A-1-(20.00)